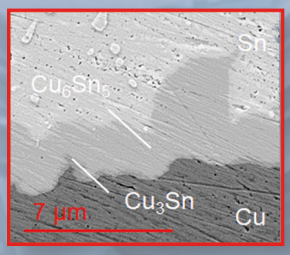
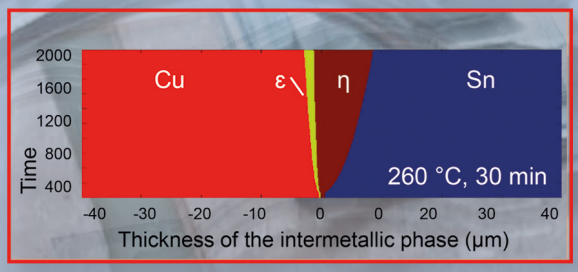
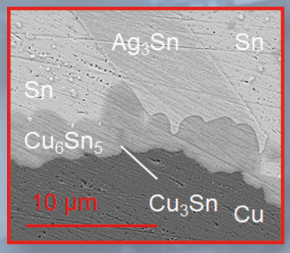
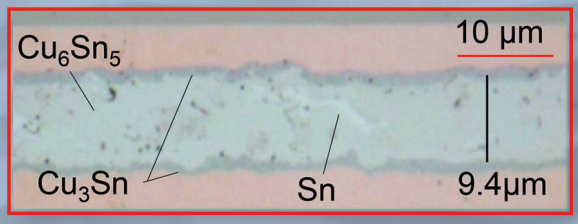








FAU Studien aus dem Maschinenbau 315

Aarief Syed-Khaja

Diffusion Soldering for High-temperature Packaging of Power Electronics

FAU UNIVERSITY PRESS

Aarief Syed-Khaja

Diffusion Soldering for High-temperature Packaging of Power Electronics

FAU Studien aus dem Maschinenbau

Band 315

Herausgeber der Reihe:

Prof. Dr.-Ing. Jörg Franke
Prof. Dr.-Ing. Nico Hanenkamp
Prof. Dr.-Ing. habil. Marion Merklein
Prof. Dr.-Ing. Michael Schmidt
Prof. Dr.-Ing. Sandro Wartzack

Aarief Syed-Khaja

Diffusion Soldering for the High-temperature Packaging of Power Electronics

Dissertation aus dem Lehrstuhl für Fertigungsautomatisierung und Produktionssystematik (FAPS)
Prof. Dr.-Ing. Joerg Franke

Erlangen
FAU University Press
2018

Bibliografische Information der Deutschen Nationalbibliothek:
Die Deutsche Nationalbibliothek verzeichnet diese Publikation in der Deutschen Nationalbibliografie; detaillierte bibliografische Daten sind im Internet über http://dnb.d-nb.de abrufbar.

Bitte zitieren als

Syed-Khaja, Aarief. 2018. *Diffusion Soldering for High-temperature Packaging of Power Electronics.* FAU Studien aus dem Maschinenbau Band 315. Erlangen: FAU University Press. DOI: 10.25593/978-3-96147-163-8

Das Werk, einschließlich seiner Teile, ist urheberrechtlich geschützt.
Die Rechte an allen Inhalten liegen bei ihren jeweiligen Autoren.
Sie sind nutzbar unter der Creative Commons Lizenz BY-NC.

Der vollständige Inhalt des Buchs ist als PDF über den OPUS Server der Friedrich-Alexander-Universität Erlangen-Nürnberg abrufbar:
https://opus4.kobv.de/opus4-fau/home

Verlag und Auslieferung:
FAU University Press, Universitätsstraße 4, 91054 Erlangen

Druck: docupoint GmbH

ISBN: 978-3-96147-162-1 (Druckausgabe)
eISBN: 978-3-96147-163-8 (Online-Ausgabe)
ISSN: 2625-9974
DOI: 10.25593/978-3-96147-163-8

Diffusion Soldering for the High-temperature Packaging of Power Electronics

Diffusionslöten für die Hochtemperatur Packaging der Leistungselektronik

Der Technischen Fakultät
der Friedrich-Alexander-Universität
Erlangen-Nürnberg

zur
Erlangung des Doktorgrades Dr.-Ing.

vorgelegt von

Aarief Syed-Khaja, M.Sc.

aus Tanuku, Indien

Als Dissertation genehmigt
von der Technischen Fakultät
der Friedrich-Alexander-Universität Erlangen-Nürnberg

Tag der mündlichen Prüfung: 04.12.2017

Vorsitzender des Promotionsorgans:	Prof. Dr. –Ing. Reinhard Lerch
Gutachter:	Prof. Dr. –Ing. Jörg Franke Prof. Dr. rer. nat. Bertram Schmidt, OvGU Magdeburg

Preface

The present dissertation originated during my work as a research associate at the Institute for Factory Automation and Production Systems (FAPS) at the Friedrich-Alexander-Universität Erlangen-Nürnberg in Germany.

I would like to thank Prof. Dr.-Ing. Jörg Franke, the chairman of the Institute FAPS, and the first reviewer of this dissertation, for the scientific freedom, benevolent support and the trust given to me for carrying out this work. I would also like to sincerely thank him for taking over the presidency during my doctoral examination. Prof. Dr. rer. nat. Bertram Schmidt, the chairman of Chair Microsystem Technology at the Institute for Micro- and Sensor Systems (IMOS) at the University Magdeburg, I thank for his support as second reviewer for the doctoral thesis. I also would like to thank Prof. Dr.-Ing. Martin März, the chairman of the Chair for Electrical Power Engineering (LEE) at FAU Erlangen-Nürnberg for acceptance as member of the examination committee. The dissertation relies as part of the results achieved in context of funded projects. For the funding is to thank the Federal Ministry of Education and Research (BMBF).

I would like to thank all my colleagues, especially at the electronics production group at FAPS, for the productive cooperation, the constructive discussions, the great willingness to help and the support in the numerous projects. I would like to emphasize in this context mainly Christopher Kästle, Martin Müller, Dr. Andreas Reinhardt, Denis Kozic, Dr. Rene Schramm, Johannes Hörber, Stefan Härter, Gerald Gion, Alireza Esfandyari and my student assistants. My many thanks also goes to the Michael Pfeffer, Thomas Kuhn, and Dr. Christian Goth for their contributions at the Institute. My special thanks goes to Dr. Markus Detert from IMOS, Magdeburg for his ever encouraging discussions towards my professional goals. For the collective experimental work and contributions on the diffusion soldering technology, I thank Dr. Alexander Klemm from IAVT, Technical University Dresden and Dr. Dean Hamilton from the University of Warwick.

Last but most important, my heartfelt thanks go to my family, especially my parents and my sister. Thanks to their ongoing consideration and support, they have made the successful completion of this work possible.

Nuremberg, in March 2017 Aarief Syed-Khaja

Table of contents

List of Symbols and Abbreviations

Symbol	*Unit*	*Description*
m_{ACu}	kg	Atomic mass copper
m_{ASn}	kg	Atomic mass tin
p_a	Pa	Atmospheric pressure
pc	%	Fraction oft he copper particles in total volume
t_H	s	Hold time in solder temperature profile
t_L	s	Soldering time in solder oven
t_W	s	Waiting time in the solder oven
t_A	s	Annealing time in solder temperature profile
t_P	s	Peak time in solder temperature profile
V_{Solder}	m^3	Volume of the solder material
V_{Void}	m^3	Volume of the void in the solder material
w_{Cu}	%	Mass fraction of copper in total metal mass
ΔT_C	K/s	Cooling gradient
ΔT_H	K/s	Heating gradient
η_F	Pa.s	Viscosity of a fluid
T_p	°C	Peak temperature in solder profile
T_H	°C	Holding temperature in solder profile
T_S	°C	Solder temperature in solder profile
ρ_{Cu}	kg/m^3	Copper density
ρ_F	kg/m^3	Density of a fluid
ρ_P	kg/m^3	Density of a gas bubble in fluid
$\rho_{SnCuo.7}$	kg/m^3	Densiity of composition $Sn_{99.3}Cu_{0.7}$
φ_c	%	Volume fraction of copper particles
φ_{Cu}	%	Volume fraction of copper in total metal volume
d	m	Mean solder bondline thickness
f	%	Packing density
g	m/s^2	Acceleration due to gravity
p	Pa	Pressure in a gas volume/ bubble
P	%	Final void percentage
R	m	Radius of a gas bubble in a fluid
T	K	Temperature
V	m^3	Volume
α	°	Angle of inclination of the chip

γ	N/m	Surface tenstion
Δp	Pa/s	Pressure gradient
Π		Pressure ration

Abbreviation	***Description***
CAPM	Cold Active Plasma Metallization
CFL	Conductive fluxless
CNR	Contrast to noise ratio
CTE	Coefficient of thermal expansion
DCB/DBC	Direct copper bonded/ Direct bondable copper
EDX	Energy dispersive X-ray
GaN	Gallium Nitride
HEMT	High electron mobility transistors
HMM	High melting material
IGBT	Insulated gate bipolar transistor
IMC	Intermetallic compound
IMP	Intermetallic phase
IOT	Internet of Things
LMM	Low melting material
LTS	Low-temperature sintering
MOSFET	Metal-oxide-semiconductor field effect transistor
OPC	Overpressure convection
PDP	Plasmadust process
PTT	Post thermal treatment
SEM	Scanning electron microscopy
SiC	Silicon carbide
SLID	Solid Liquid Inter-diffusion
TLPB	Transient liquid phase bonding
TLPS	Transient liquid phase soldering
VVP	Vacuum vapor phase soldering
WBG	Wide bandgap
WPC	Work piece carrier

1 Introduction

The world and the people's lives are being continuously revolutionized by the concepts of digitalization and electrification. The mindset and goals of governmental, academic and industrial organizations are greatly influenced by the megatrends like electro-mobility, healthcare and renewable energy in the quest for efficient and sustainable solutions. In this era of fourth industrial revolution (Industrie 4.0), every interface in the manufacturing technologies is being supported by electronics enabling high level of automation and data exchange starting from the customer requirements over product design to delivery and customer feedback. These hold true irrespective of the type of product or the industry. In this context, various business models and product designs are being continuously modified to add value and often new functions by means of digitalization to enable energy savings and cost reduction.

More than 40% of the days overall global energy consumption is electrical energy and this proportion is expected to rise to 60% until 2040 [1; 2]. One of the key enabling technologies in the way to a more sustainable world is 'power electronics' besides electrical energy storage. The European Union's ambitious climate goals for the reduction of energy consumption and CO_2 emissions cannot be achieved without the extensive use of power electronics. About 30% of the electrical energy consumption can be saved by consistently using power electronics with standard efficiency levels above 95% for the power conversion [3; 4]. Largely driven by the electric and hybrid vehicles markets next to energy sector, the power electronics market value will surpass $17 billion by 2020 supported by a $4 billion value raise by the proliferation of 'Internet of Things' (IoT) products and new generation electrical vehicles [5; 6].

Power electronics is the key technology associated with efficient conversion, control and conditioning of electric power from its available input into the desired electrical output form. Digital power electronics holds the key for effective generation, distribution and use of electrical energy by efficient transmission and control. It is a cross-functional technology covering from the very high gigawatt (GW) power (e.g. energy transmission) down to the very low milliwatt (mW) power (e.g. mobile phone operation). According to the application areas, the devices should be capable of operating under extreme ambient conditions depending on the power levels and heat dissipation. Temperatures for example can reach up to more than 150 °C in conventional silicon (Si) based power modules leading to failures

due to the component itself or the used packaging technologies. A significant research is required to address the ever increasing power densities in silicon based power electronics and related thermal management requirements.

The new generation wide-band gap (WBG) semiconductor devices like silicon carbide (SiC) and gallium nitride (GaN) are being developed to overcome the limitations of Si. Here compared to silicon counterpart higher power densities are realizable in even smaller sizes of the components where the junction temperatures of devices can elevate to more than 400 °C and in the assemblies to more than 300 °C [7; 8; 9; 10]. On the other hand accompanied with compact WBG devices, there is a growing trend towards miniaturization in power electronic systems for high system integration enabling reduced system volume and cost, improved efficiency, enhanced system functionality and performance [3; 11]. This is a key driver in industry particularly in physical design of the product, where over-design results in additional volume, weight and in few cases manufacturing and assembly costs, increasing the cost of the final product. The main hurdle in this case is the increase of power densities at all the packaging levels.

There are various approaches to increase the power density in a power electronic module, mainly by the improvement of cooling system (i.e. removing higher power dissipation to keep the semiconductor at optimal efficiency level), improvements of power electronic components (i.e. reducing power losses) and, increase of operating temperatures of the individual components of the module near to heat dissipating components. For the third approach, it is required to optimize the packaging technologies around the component specifically backside i.e. die-attach, and frontside (e.g. wire-bonds) interconnections capable of sustaining high thermo-mechanical stresses and operating at high temperatures with good thermal and electrical performance.

Irrespective of the approach considered, the interconnection technology used in the power module mainly die-attach has a direct impact on the lifetime of the module. The soft-solder based state-of-the-art Si-based power packages are presently limited by temperature sensitive packaging concepts and insufficient heat dissipation [12; 13; 14; 15]. Removing heat is also critical to the operation and long-term reliability of the power modules. Cooling solutions however directly add weight, volume, and cost to the product, without delivering any functional benefit. Similarly production of cost-effective, high-quality and reliable modules in this perspective depends on the proficiency in the electronics packaging. In this context, a

high-temperature die-attach technique is to be designed to mainly address the requirements of new generation power electronic components and modules. This technique should be economical with low investments, low-cost materials and also highly customizable for the new product designs.

Objectives of the Thesis

Lead-free soldering of bare-dies to substrate and substrate to baseplates or interposers still dominates the power electronics industry. The high-temperature interconnection techniques using gold-based active solders or silver (Ag) materials for sintering are already in production, however are associated with intricate production equipment and are limited to very few designs due to cost factors [16; 17; 18]. Diffusion soldering technology is a well-known interconnection technique, where high-remelting intermetallic phases (IMP) are produced between two high melting metals (HMMs) through interdiffusion process by using a low-melting material (LMM) as interlayer [19]. The scientific and technological objective of this thesis is the development and optimization of diffusion soldering technology as a low-temperature interconnection technique for a stable high-temperature operation in power electronic applications. The variant of diffusion soldering, namely Transient Liquid Phase Soldering (TLPS) has been investigated. The economic and social objective is to lower the manufacturing costs and portability for integrating TLPS with high flexibility and customization into the presently available production infrastructure without additional investments. For this, the state-of-the-art and advanced soldering techniques were investigated in detail with thermal and pressure profiling for full intermetallic phase (IMP) transformation and high quality i.e. low-void percentages and process-generated defects. These were performed with variations in substrate materials, semiconductor chip metallization, and interlayer materials. With respect to the production of power modules with TLPS as die-attach, the conventional process-chains are to be optimized for high-quality and reproducibility of reliable and defect-free TLPS interconnections. These demands also for the optimization of the state-of-the-art power electronic production process-chains with other new assembly technologies for the economical production of this high-temperature interconnect technology.

Organization of the Dissertation

This thesis is divided into ten chapters. In the second chapter, the state-of-the-art technologies with respect to the semiconductor materials, construction and packaging, and the corresponding trends prevailing in power electronics are described through roadmap analysis. Parallelly the results of a world-wide survey with 143 participants performed through the Institute FAPS as part of the work are also summarized. An overview on the advancements of the interconnection technologies and their high-temperature variants are explained and summarized with an outlook to diffusion soldering.

Further in third chapter, the theory behind diffusion soldering and its variant mainly TLPS technology is described. A detailed overview on the mechanism and process conditions for TLPS is given to elaborate the process complexities of the present approaches outlining the research methodology followed in this work. A short synopsis is also given on the methodologies followed in this thesis work to realize this high-temperature stable interconnection technique. The influential factors for defect-free TLPS are sketched into an Ishikawa diagram.

Chapter four introduces primarily the machines and analysis equipment used in the work followed by the contribution in the material development mainly copper-tin (Cu, Sn) based solder pastes and fluxless preforms. In chapter five, the investigations performed for the procurement of the interconnection layers mainly for paste-based and cold-active plasma metallization (CAPM) enhanced TLPS process development are outlined. Here the results obtained in the development of the stencil printing process for solder layers down to 20 µm are also summarized.

In chapter six, firstly the concentration gradient based simulation of the Cu-Sn bimetallic diffusion process for estimating the influences of temperature and time is introduced. This is followed by preliminary experimentation and an extensive analysis of the obtained IMP thicknesses for the verification of simulation results. The primary investigations on the voiding characteristics of the various temperature profiles with void-reduction concepts of vacuum and over-pressure for thin solder layers as basis for obtained void-free paste- and preform-based TLPS are introduced. This is followed by the interpretations through In-situ X-ray investigations performed parallelly to optimize the TLPS process.

In chapter seven, the extensive work performed in the optimization of the soldering approach for the TLPS process for a reliable and economic production is detailed. The influences of the materials mainly the interlayer, semiconductor metallization and substrate surface finish on the voiding characteristics, void percentages and IMP growth with respect to the type of temperature and pressure profile are discussed. The void formation and IMPs are evaluated for produced TLPS joints and the successful realization of the methodologies and selection of profile parameters are illustrated. The defects observed for the produced interconnects are discussed and compared for evaluating the joint quality by means of room- and high-temperature shear tests. The chapter is summarized by the temperature cycling results.

In chapter eight, a demonstration of the developed approaches through product and technology case studies is shown. A power electronic module had been developed using preform-based TLPS approach as product case study. The developed profiles were tested for the TLP Bonding for Cu-Sn and Ag-Sn systems as technology case study. The chapter is concluded with outlook on new material combinations, machine enhancements and process profiles for reliable TLPS interconnects with high level of flexibility and customization. The chapters nine and ten conclude the thesis work summarizing the results of the followed TLPS strategies and outlook for the production of power electronics with this low-temperature interconnection technique for high-temperature packaging in power electronics.

2 State-of-the-art Technologies and Trend Analysis

2.1 Overview of Power Electronics Modules

Power electronics is often provided in form of power electronic modules or systems consisting of semiconductor components. The main tasks are to convert, manage and recycle the electric power efficiently. The conversion of electrical power is required in e.g. inverters, rectifiers and DC-DC converters in various applications. The next two tasks of managing and recycling are found in the applications of power throttle and stabilization [3; 20; 21]. The semiconductor components basically could be controllable transistors or thyristors and non-controllable diodes. The selection of the switching elements for power electronic applications is mainly based upon current-carrying capability in the ON-state and the maximum blocking voltage next to the switching frequency.

The construction and interconnection technologies used in a power module are substantially determined by functional requirements such as the operating voltage, the current-carrying capacity or the switching frequency. Generally a high level of system integration for compactness, low-cost and shorter process chains is required [22]. Due to the fact that, monolithic integration of the power electronics in a single chip (Level 1) is generally not feasible, the System-in-Package (SiP)[1] concept of hybrid integration (Level 1) with modern packaging and interconnection technologies (Level 2) plays a very important role. The crucial task of packaging is the protection against environmental influences and stresses such as temperature, humidity or vibration, being thermally, electrically and mechanically stable during the duration of operation. These tasks can be grouped as:

- ensuring a mechanical cohesion and electrical interconnection
- providing electrical and thermal isolation
- dissipation of heat developed due to power losses
- protection against harmful environmental conditions

[1] System integration concept: Level 0 - Intellectual Information, Level 1 - Electronic Element, Product Level 2 - Electronic Package, Product Level 3 - Electronic Module, Product Level 4 - Electronic Unit, Level 5 - Electronic System

- interface to the periphery of the overall structure (application dependent)
- ensuring the required or demanded lifetime

The interconnections and housing are generally designed taking into account the aforementioned requirements that the tasks are best fulfilled in the context of the technical specifications. These in the power electronic module development can be categorized into three levels of interconnect or packaging as explained below:

- **Top-level interconnect** (Level 2 to Level 1 i.e. carrier substrate to chip frontside or Level 1 to Level 1 i.e. chip frontside to the next chip frontside)
- **1st level interconnect** (Level 1 to Level 2 i.e. chip backside to the carrier substrate or also chip frontside to a second carrier substrate)
- **2nd level interconnect** (Level 2 to Level 3 i.e. carrier substrate to the base plate or interposer or heat sink)

In case of the carrier substrates, the isolation of high currents in copper conductors with other parts of the module is provided by ceramic materials like Al2O3, Zirconia toughened Al_2O_3, AlN or Si_3N_4 in form of ceramic circuit carriers like direct copper bonded (DCB) or active metal brazed (AMB) substrates depending on the application [23; 24; 25; 26]. The lead-free Sn-based soft solders are regular interconnection materials generally of Sn-Ag-Cu or Sn-Ag compositions. The main aim of the packaging at levels of 2, 3, and 4 is the effective heat transfer of the mounted semiconductor die with good thermal conductivities. The state-of-the-art technologies in cases of the semiconductor components, substrate and interconnection materials are summarized in the following sub-chapters. The first and second level interconnects are generally constructed as in Figure 1. In case of power modules with very high power densities and heat dissipation, the top-level wire-bonds are replaced with soldered metal terminals or DCBs for double-sided passive or active cooling of the assemblies. The assemblies either soldered or bonded through thermal interface material (TIM) to the base plate or heatsink. In few customized modules to reduce the problems with wire bonding and increase flexibility, press-pin or spring contacts are also used with direct electrical connections without any bonding material [20]. The conventional power modules comprise of semiconductor component to form a basic rectifier or converter circuit. The selection of design i.e. module size and materials depends on the application and also on the heat generating components.

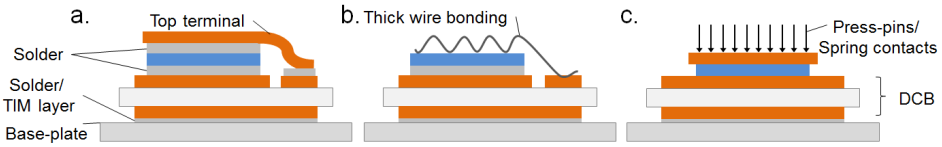


Figure 1: Packaging of semiconductor components in power electronic modules; a. two-sided soldered; b. Frontside thick wire-bonded and backside soldered; c. Pressure contacting using press-pins or spring contacts. Reproduced from [20].

For modules with high-power densities, an interposer or a base-plate is essential to uniformly dissipate the thermal losses from the semiconductor components to heat-sink. Increase in heat spreading area i.e. the copper conductor thickness of the substrate under the chip results in faster conduction of heat enabling higher currents through the chip. For simpler design and easier module replacement, mountable press-pin packages without baseplates are also used.

The module designs with or without baseplate can be seen in Figure 2. The semiconductor, top-level interconnections, and substrate surface are covered by soft encapsulation materials and in few cases followed by hard encapsulation. The package type and size depends on the intended function of the module and number of mounted semiconductor components. The materials used in the assembly of a power module with base-plate design are shown in Table 1.

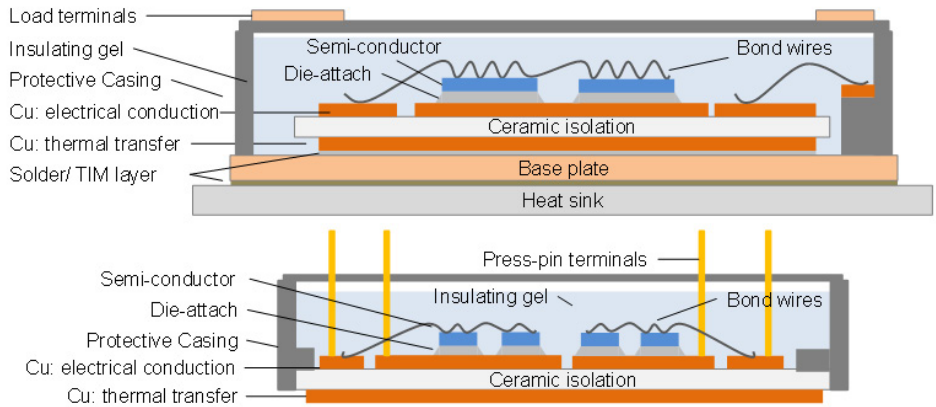


Figure 2: Schematic structure of a typical base-plate power module (top) and press-pin package (bottom) showing various levels of interconnects.

Table 1: Material and thickness specifications of a typical DCB-baseplate module

Structure layer	Materials used	Thickness (µm)	Level	Cross-section
Bond-wires	Al, Cu, Al- cladded	300 - 500	1-1, 2-1	
Semiconductor	Si, SiC, GaN	80 - 250	1	
Die-attach	Sn-based soft solders	70 - 120	2-1	
Substrate	Cu/ ceramic/ Cu	~ 330/ 330/ 330	2	
Solder/TIM	solders/ thermal	100 - 150	2-3	
Baseplate	Ni-plated Cu	3000	3	
TIM	Thermal paste	< 100	3-4	
Heatsink	Al, Cu, AlSiC	-	4	

A continuous development of construction and interconnection techniques can be seen from last three decades from the power-electronic module manufacturers for discrete one-component or multi-component packages [20; 22]. The height of the package is generally defined depending on the wire-bond loop height i.e. 2 - 4 mm or the used top-side metal terminals than the solder heights of less than 150 µm. Various package types and packaging techniques can be seen in Figure 3 and Figure 4. Numerous concepts for reducing the height for compact system integration and intelligent power modules were continuously researched in the last decade and upscaled to production. These technologies are termed depending on the technology and the application e.g. namely SiPLIT technology (Siemens) [27], Blade-package (Infineon) [28], and SKiN technology (Semikron) [18; 29]. In case of SiPLIT and Blade packages, the conventional wire-bonds are replaced by the copper galvanization and corresponding pattern structuring for isolation materials. Though the process is complex compared to wire-bonding, the goal was to achieve high system integration and design freedom together with high level of automation. In case of SKiN technology, the large-area structured copper contacts in form of foils are connected to frontside of the semiconductor. The conventional wire-bonding and soldering were replaced with Ag-sintering technology to achieve high reliability and flexibility with thermal design and product customization [30].

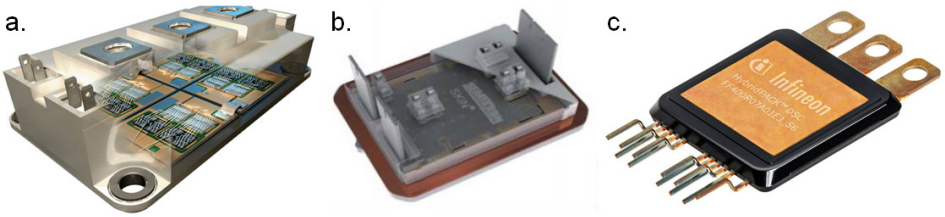


Figure 3: Power module types showing various terminal concepts a. Conventional base-plate [31]; b. SKiN power module [18; 29]; c. HybridPACK DSC package [32].

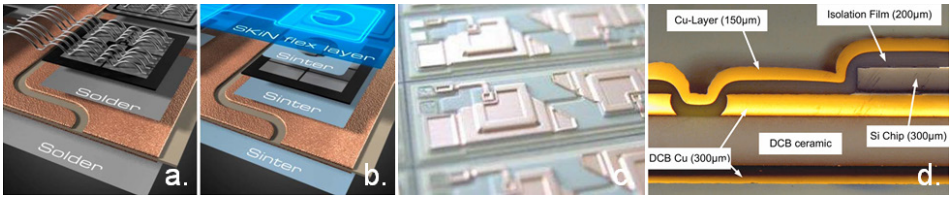


Figure 4: Comparison of top-level interconnects a. conventional wire-bonded module; b. SKiN technology with Ag-sintered Cu-flex top-interconnection [18; 29]; c,d. SiPLIT technology with Cu-galvanic metallization with isolation layer [27].

Next to conventional power module concepts, the COOLiR2 and HybridPACK technologies with double-sided cooling (DSC) are marketed from the companies International Rectifier and Infineon respectively [32; 33]. Here both sides of the semiconductor are soldered to either DCBs or copper terminals for better yield and reliability. Most of the above concepts are already in serial production for various applications. The high-temperature packaging alternatives are discussed in next sub-chapters. Further innovative technologies and concepts for increasing the power densities and WBG integration are also available under market names GE power overlay [34], Delphi Viper [35], agile Power Switch 3D-Integration (aPSI3D) [36] and double sided cooling modules for Lexus LS600H and PRIUS 2010 [37].

2.2 Technological Trend and Roadmap Analysis

Preliminarily the latest roadmaps mainly the ECPE 2025 Roadmap [6; 38], ZVEI Trends 2022 [39], iNEMI Technology Roadmap 2015 [40; 41] and 2015 IPC Technological Roadmap for Electronics Interconnects [42] were analyzed to understand the technological trends and requirements for the packaging of power electronics. As part of this thesis work, to understand the requirements and specifications of the power electronic industry, a detailed worldwide survey with focus on packaging and production technologies was conducted. The interpretations from the roadmaps were used to create a detailed questionnaire. This included 15 English and German-translated questions regarding semiconductor materials, interconnection

techniques and materials, application specific requirements, production technologies followed and future trends. Though the post-survey analysis was extensive, only the relevant interpretations for high-temperature packaging related to this thesis are summarized in this section. Other perspectives of power electronic design, topologies, or functionality are not focused. The survey questionnaires created through online survey platform 'SoSciSurvey' were sent to more than 350 industrial and academic contacts directly or through academic networking groups. A response from total of 143 participants from 19 countries was obtained as shown in Figure 5. The survey was active online and the results were collected over a time period of 5 months from June to Oct 2015. It can be observed that the European participants geographically and industry participants organizationally dominated the conducted survey.

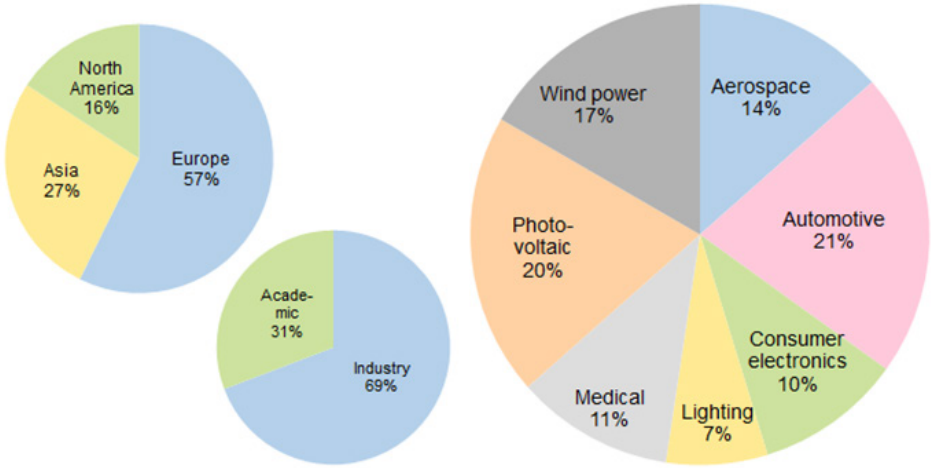


Figure 5: Geographical, organizational and market distribution of the survey participants (left to right).

2.2.1 Evolution of Semiconductor Materials

In power electronics, there is no specific reference like 'Moore' law'[2] as in microelectronics due to restrictions of conductivities and thermal limits. As there is no new concept of passives, the power electronic components are dependent on the progress in material sciences. Silicon has been the dominant semiconductor material since its replacement of germanium.

[2] Moore's Law predicts that the density of components in integrated circuits doubles every year [43]

Though a continuous improvement of Si devices can be seen since past three decades [44], these are limited to low operating temperatures less than 120 °C due to material intrinsic properties limiting the capability and efficiency of power semiconductor systems. This is also limited partially by the packaging technologies [12; 45].

Wide-band gap (WBG) power semiconductors especially SiC and GaN, which have the capabilities of higher switching frequencies, higher operating temperatures and higher blocking capacity, are slowly penetrating into various market segments [20; 46; 47]. The main drivers for the WBG integration are the reliability, reduced parasitics, power density and stable high-temperature operation in a packaging perspective [47]. SiC devices are expected to dominate the upper voltage class greater than 1200 V and GaN devices for lower voltage classes less than 600 V. Apart from the advantages offered by WBG materials, an important challenge is the packaging of the components for high temperature operation mainly in the die-attach systems to reduce the loading on the top-level interconnects and to run the system at optimal efficiency [48; 49; 50; 51]. An overview of the properties of the conventional Si and new generation WBG materials like SiC and GaN is shown in Figure 6 with respect to the key material properties. The WBG materials have significantly higher energy bandgap compared to silicon, which results in lower switching and transmission losses, higher chip temperatures and a better thermal conductivity. This enables the potential and advantages of WBG materials for high-voltage, high-frequency and especially high-temperature applications [20].

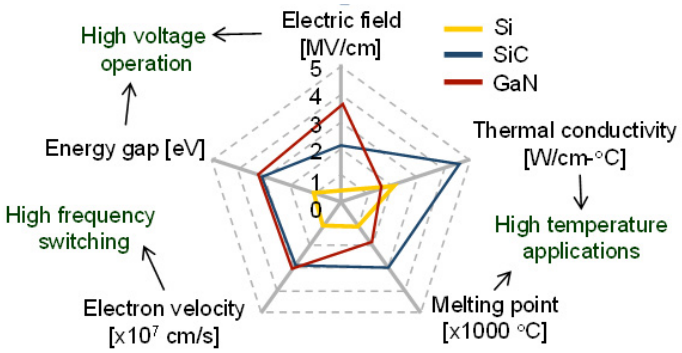


Figure 6: Comparison between key material properties SiC vs Si vs GaN.

The semiconductor density also plays a major role in further development of power modules. Here the increase of power density through WBG i.e. achieving the same characteristics, only by using a fraction of semiconduc-

tor material i.e. smaller component dimensions compared to silicon increases hugely the power dissipation in a small volume. The module design is to be accordingly optimized to achieve a high level of system integration without reducing the efficiency or performance.

The Figure 7 shows the results of the survey conducted on the relevance of the semiconductor materials. It can be observed that silicon will prevail in most of the applications in the next 10 years. However the SiC and GaN also will penetrate into various applications with increasing relevance in industrial or private-sector companies. The new WBG based combinations such as GaN-on-Si and GaN-on-SiC, however seems to be partially relevant presently and in the next 10 years compared to GaN semiconductor material.

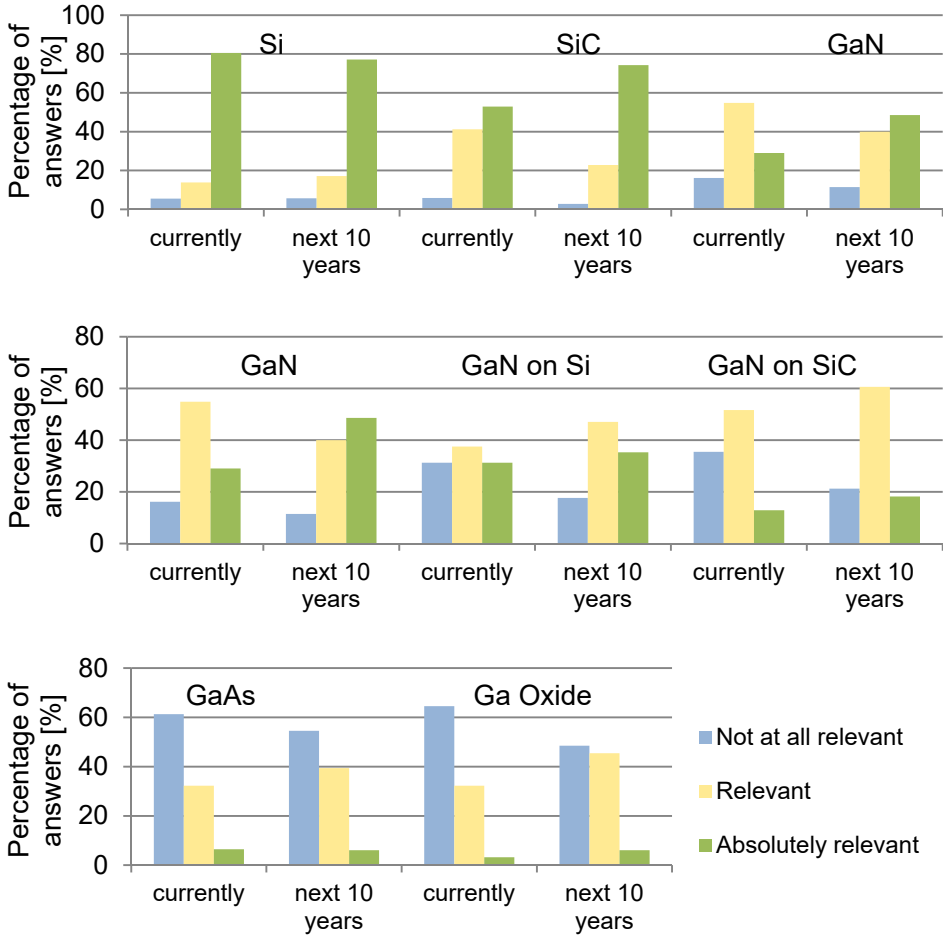


Figure 7: Relevance of semiconductor materials now and in next 10 years for a. Si, SiC and GaN; b. GaN, GaN on Si and GaN on SiC; c. GaAs and GaO.

The responses from the industrial participants however indicate that the materials as GaAs and GaO are not at all relevant at present or in next 10 years. Based on the organizational distribution, the materials as GaAs, GaO, InGa, Carbon, Diamond and organic semiconductors will be researched in academic institutions in the next 10 years

2.2.2 Roadmap Analysis and Technological Survey at FAPS

Various roadmaps were analyzed namely 2015 iNEMI, 2015 IPC, ECPE Power electronics 2025, ZVEI until 2022 for the requirements and trends [40; 38; 52; 42]. These mutually agree on the increasing requirements of the industry and summarize to reliability issues, demand for standards, high temperature capability, thermal management requirements, system integration, demand for simulation, packaging and interconnection technologies. Irrespective of the roadmap analyzed, the main trend evaluation factors depend on the application-based drivers and the key performance indicators (KPIs) at various levels like converters and systems. Below are the requirements according to the application from the iNEMI Roadmap:

- Consumer electronics: small size (volume), costs and functionality
- Automotive applications: overall costs and reliability
- Aerospace applications: reliability and environmental influences
- Industrial electronics: long lifetime and reliability
- Medical applications: security and conformity (standards)
- Wind power and industrial drives: reliability and resistance against environ-mental influences

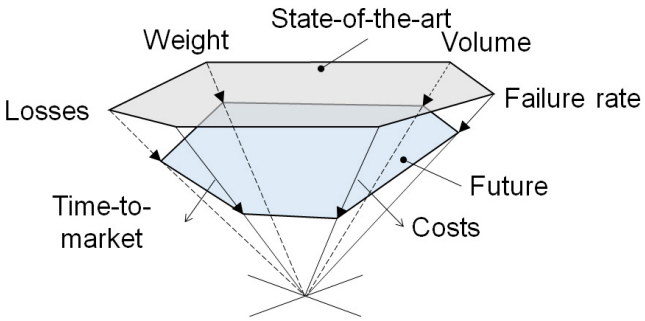


Figure 8: Key performance indicators according to the ECPE Roadmap 2025. [6]

An overview of the KPIs used in recent years at module level is shown in Figure 8. The KPIs directly linked to the packaging and interconnection technologies are the failure rate and costs, however the others as volume

and weight also have an indirect influence and can be considered as secondary KPIs. Regardless of the application, the main requirements are the reliability of the product i.e. lifetime requirements and the overall costs particularly for consumer and automotive sectors.

The above mentioned KPIs have been transformed into more meaningful new KPIs as part of ECPE 2025 Roadmap [6; 52]. These however give a different meaning to the importance of the packaging and interconnection requirements. These are mainly power density [kW/dm³] [3], power per unit weight [kW/kg] [4], relative costs [kW/$] [5], relative losses [%] [6], failure rate [h^{-1}] [7]. Based on these proposed KPIs, the survey revealed the following results as shown in Figure 9.

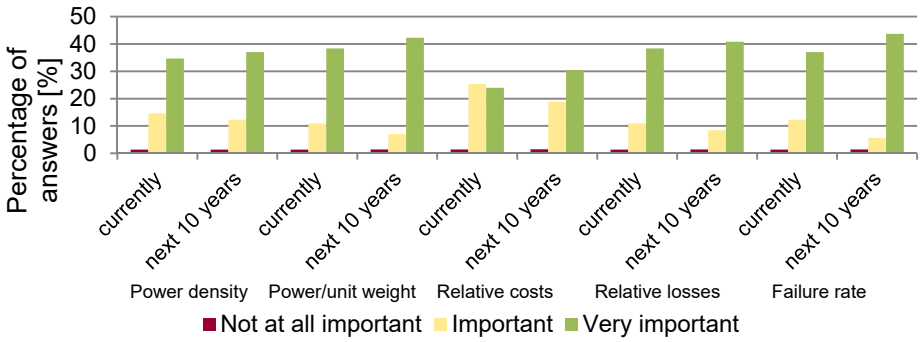


Figure 9: An overview of the survey answers on the importance of the KPIs.

It was observed that all the KPIs had maximum importance in industrial and academic institutions. The 'relative costs' however was opted as intermediate importance from aerospace sector industries. Along with these

[3] Power density is a factor that shows the amount of power that is possible through a specific amount of volume. The factor can also reveal the amount of volume that is necessary to fulfill the required power needs. The factor is described as amount of power in kW per dm³ (volume unit).

[4] Power per unit weight is a factor that shows the amount of power that is possible through a specific amount of weight. The factor can also reveal the amount of weight that is necessary to fulfill the required power needs. The factor is described as amount of power in kW per kg (weight unit).

[5] Relative costs is a factor that shows the amount of power that generates a specific amount of costs. The factor is described as amount of power in kW per $ (monetary unit).

[6] Relative losses is a factor that shows the percentage of losses based on a potential optimum of converter losses of 0 %, which would indicate 100 % efficiency.

[7] Failure rate is a factor that shows the number of occurring converter failures in a specific time. The factor is described as number of failures per h (time unit).

KPIs, the module requirements for high-temperature operation, robustness, reliability, environmental impact, and weight reduction were accompanied as supporting arguments from the participants.

The ZVEI Roadmap also indicates this through two important trends in the future [39]. One important trend linked to relative or development costs is in the field of rapid prototyping and flexibility for packaging and interconnection technologies. Another trend was the development of packaging and interconnection technologies for miniaturized modules and for tight connected structures which focuses on the high-temperature operation, increased power density and lifetime.

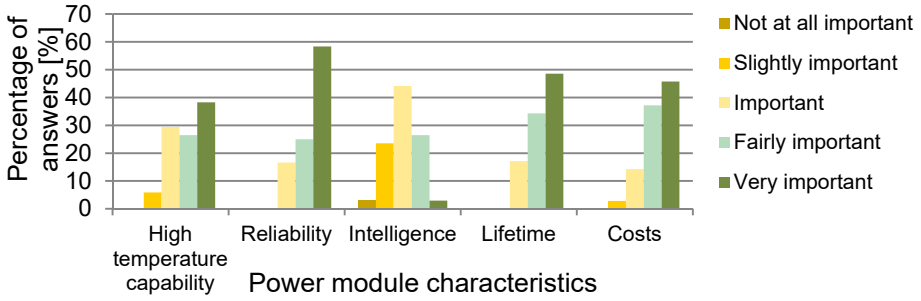


Figure 10: The importance of the power module characteristics.

As shown in Figure 10, the same is indicated on the required power module characteristics. The integrated intelligence is indicated as partial importance, however the other KPI influential factors are given more importance. An intermediate importance is given to the simulation tools and topologies as can be observed from Figure 11 on the technological trend focus. These include the simulation requirements for the multi-criteria failure mechanisms involving various failure modes with different types of loading and material combinations.

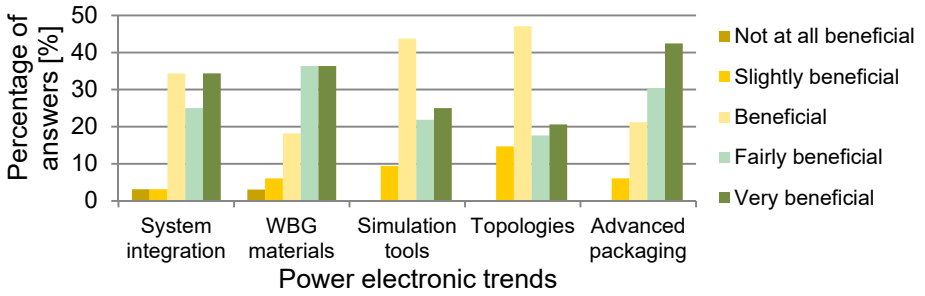


Figure 11: An overview of the relevance of the technological trends to power electronics manufacturers in packaging perspective.

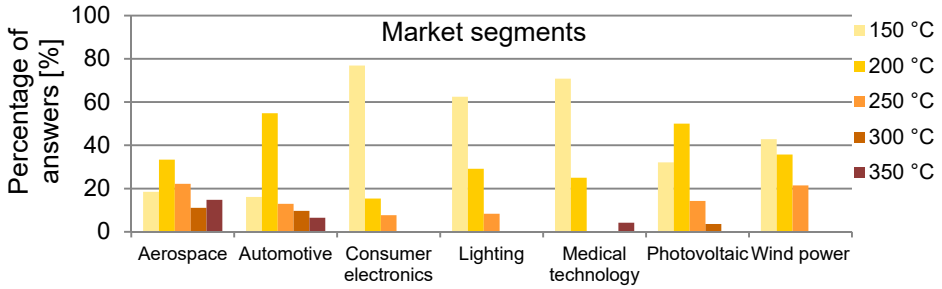


Figure 12: Temperature requirements in different market segments.

The participants also agree with the three key trends of system integration, WBG materials and advanced packaging. The topology changes are not considered relevant for WBG materials as long as the other trends are still in research and development. Increasing requirements for the packaging and interconnection technologies are evolving as the application spectrum is growing significantly.

In Figure 12, the automotive and aerospace sectors have new integration concepts where the temperatures could rise to more than 250 °C and various maintenance restrictions have to be considered. Examples in these sectors can be the engine compartment and on-engine or on-transmission component placement. As responded by the participants, the packaging requirements with respect to temperatures in fields of industrial and motor drives are 200 °C, integrated motor and integrated motor drives, oil and gas exploration are 300 °C, military, energy and space exploration are 350 °C. The resulting technological requirements in the field of electrical and thermal loading capabilities are valid for packaging and interconnection technologies as an adaption of the production processes is needed to create devices that are able to withstand these conditions. Another indicated important criterion linked to the lifetime and failure rate is the ageing process of material with temperature and stresses.

Concerning lifetime requirements, the expectation for consumer electronics changes for 5 years from currently '5K-10K operation cycles' to more than '10K operation cycles' in 2020. For portable industrial and automotive products, the current expectation of more than '10K operation cycles for 15 years' will remain valid in 2020. Industrial and automotive applications which belong to the product board have currently a life expectation of 10 years with more than 10K operation cycles which will also be valid in 2020. The lifetime expectation of portable medical products remains 5K-10K operation cycles over 10 years in 2020. For medical products which belong to the product board the lifetime expectation of 5K-10K operation cycles

over 9 years will also not change until 2020. This has huge influence in the high-temperature operation, where heat resistant materials for the used interconnections, encapsulation are to be implemented eventually. This also true for the substrate technologies where new material combinations are searched [42].

It can be observed from the Figure 13, that the substrate technologies Direct copper bonded (DCB) and Active metal brazing (AMB) still prevail for at least 5 to 10 years in mass production. The embedded technologies however seems to integrate the market in low-voltage to medium-voltage applications in next 5 years. For high power special applications for aerospace or military, multi-layer AMB substrates with vias and backside copper slugs can be expected. The Insulated metal substrate (IMS) has high relevance in lighting sector in consumer and automotive sectors. The other substrate technologies as Thick printed copper (TPC) and Structure copper technology (SCT) however are limited to serial production for limited designs. According to organizational distribution of the participants, the Embedded technologies and TPC are to be expected in R&D for quite some years due to unanswered issues of structural integrity, thermal management and interconnection technologies.

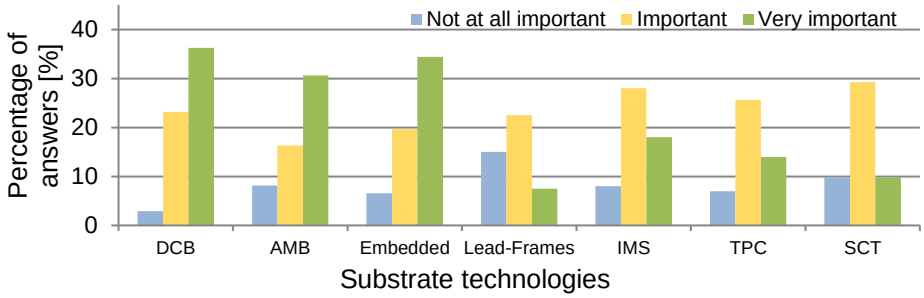


Figure 13: An overview of the importance of substrate technologies in next 5 years in power electronic applications.

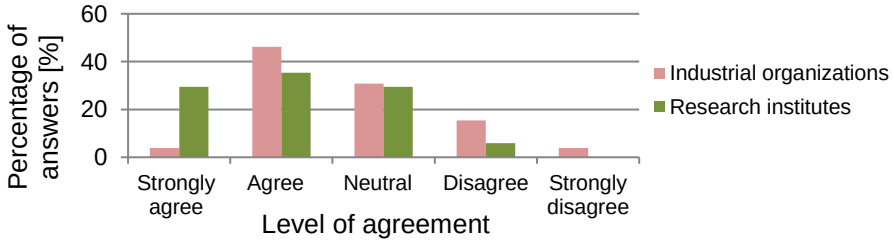


Figure 14: Level of agreement on the usage of additive manufacturing technologies in power electronics.

The IPC 2015 roadmap also found that embedding technologies as one of the main trends in the future [42]. The state-of-the-art substrate technologies are presently costly and the organizations are looking for new technologies where conductive structures can be flexibly optimizable according to the application. One such new trend obtained through the survey was the integration of additive manufacturing technologies at various levels for power electronic modules. Along with the level of agreement as in Figure 14, various perspectives were obtained with strong agreement on this future trend as follows:

1. Additive manufacturing of heat sinks (metals and ceramic materials) with embedded micro-cooling channels
2. Development of substrate technologies for product flexibility and customization
3. Rapid prototyping of printable 3D-packages based on heat-resistant materials

Furthermore as unleaded soft solders are limited in their temperature capability and reliability, challenges had to be addressed and suitable substitutes are to be searched by innovative manufacturing concepts. This is important along with ageing of materials as the lifetime of devices can be up several years depending on the application. The iNEMI Roadmap also indicates that a general understanding of ageing or degradation of materials is necessary to create a universal definition and there is a need for development as material models can be very complex in reference to the ageing influence on specific properties [40].

A current trend is the 3D wafer level packaging with high functionality per module with increased operating conditions. However this is not yet observed or implemented in power electronics due to missing technological designs or thermal management issues due to high power density and decreasing semiconductor density as in WBG materials. Current development needs are in the field of costs and process optimization. Furthermore research concerning low cost materials like Bulk Molding Compound (BMC) is necessary according to the survey. For the encapsulation materials, new materials are still in research or not yet implemented due to increased stress from the semiconductor and wire-bond materials leading to slow degradation. Minimizing the influence of packaging stress due to temperature and also moisture through intelligent layouts is of high interest according to the survey. Complex packaging and definition of the chipset will be a big challenge for the system design.

Referring to Roadmap iNEMI until 2012 the trend of packaging and interconnection technologies for miniaturized modules and for tight interconnection structures will remain valid until 2022 as the interest in further miniaturized modules and very tight connection structures will remain high. Furthermore as developments in the field of materials progress, new processes for these advanced materials are required. Other development trends are the functionalizing of modules and the integration of local intelligence and energy supply. The demand for low cost production drives the minimization of the overall product manufacturing time. It is expected that high temperature resistant solder- and sinter interconnections can be manufactured five to ten times faster in 2022. Diffusion soldering and Ag-sintering in combination with suitable high temperature capable substrate materials will increase significantly the reliability of efficient high power semiconductors. [40]

2.2.3 Summary in the Perspective of Power Packaging

This section summarizes the requirements and corresponding challenges for packaging and interconnection technologies based on the roadmap analysis and the survey conducted. The new KPIs of power electronic modules (relative costs, power density, power per unit weight, relative losses and failure rate) lead to various requirements for packaging and interconnection technologies.

First, higher power density leads to thermal management issues for interconnection technologies. To enable the required high switching frequencies that are necessary for increased power density, the packaging needs to be advanced and parasitics needs to be minimized. The corresponding temperature rise of increased power density leads to reliability issues for interconnection technologies. To improve the performance indicators advanced packaging is a key for success. The temperature capability requirement for bonding and substrate technologies will be between 200 °C and 250 °C in the future and should withstand temperature changes of 100 K. Not only should packaging and thermal management be improved for high temperature power modules, it also should be cost effective. Therefore research for low cost packaging materials is necessary and the manufacturing time should be decreased.

To support the trend of WBG semiconductors, a high temperature and low inductive package model should be developed. To apply high temperature package solutions in the industry, the manufacturing processes need to be

further developed concerning the ability to automate the production process which is mainly highlighted in this research work to bring diffusion soldering particularly TLPS technology into production.

As environmental conditions can be harsh in the area where power electronics are positioned (e.g. automotive), the packaging and interconnection technologies are mainly challenged to fulfill the reliability requirements. Therefore the production processes and materials might need to be adapted. The reliability of interconnection processes itself is also important to create reliable products. The development of materials as well as packaging and interconnection technologies should be linked very closely. On top of that, the trend of system integration and the fact that a failure can be much more severe in an integrated system increases the difficulty to fulfill quality and reliability requirements in the field of packaging. This challenge is further increased by the fact that the higher the number of integrated components, the higher is the failure probability. Furthermore sustainable package and interconnection solutions are driven by new energy policies. In addition governmental regulations are a challenge for packaging and interconnection technologies as new materials might be needed. There could be a lack of information about the reliability of these materials. The understanding of package ageing is another requirement and field of interest.

For the process of diffusion soldering, current requirements are an increased cost- and resource efficiency of the mechanism. Concerning copper wire bonding new metallization systems and corresponding bonding parameters on semiconductors are needed. Another requirement is that it should be possible to embed the new WBG semiconductors into the PCB technology, which is already in research. The application spectrum of power electronics is increasing and requirements are often application based. This leads to a challenge, that a package needs to be provided that is suitable for the right conditions. If the specific requirements are not met the device might fail or it could be overdesigned and would generate additional costs.

Overall the roadmaps and survey reveal that there exist many different requirements and challenges for packaging and interconnection technologies. The requirements are often connected with each other and highly depend on the requirements of power electronic products. The analysis of the specific roadmaps combined with the conducted survey shows that all agree on the major trends in power electronics. The information that is provided by one roadmap is extended by another roadmap as the main

focus of the roadmaps differs slightly. ECPE for example deals with all topics that are directly related to power electronics and iNEMI deals only with topics that are related to manufacturing but for the whole field of electronics. Some topics are discussed in all roadmaps. Topics that are described in most roadmaps are reliability issues, demand for standards, high-temperature capability and thermal management requirements, system integration, demand for simulation, packaging and interconnection technologies.

2.3 Requirements for High-temperature Packaging

Soldering has been dominating the electric and electronic world as interconnection technology for joining electronic components on circuit carriers. It is a thermal process carried out for securely joining of components mechanically and electrically carried out exclusively with low melting metals addressed generally as soft solder materials. The main reason for the connection is the intermetallics formed between the component, solder and conductor on the substrate carrier. Tin and lead based solders had achieved good processability and reliability over the past decades. However starting June 2006, the European Union Waste Electrical and Electronic Equipment Directive (WEEE) and Restriction of Hazardous Substances Directive (RoHS) came into effect prohibiting the inclusion of significant quantities of lead in most consumer electronics produced in the EU [53; 54]. From then, intense research had been performed to find and replace lead in solder alloys in terms of electrical, mechanical stability and long-term reliability. Additionally, the processability of these alloys must be ensured with existing manufacturing equipment in order to keep in the transition to new solders, the investment costs as low as possible. The focus however was redirected towards eutectic tin-based compositions involving mainly bismuth, copper, silver and nickel.

2.3.1 Quality Factors and Process Engineering for Harsh Environments

Concerning to the process generated defects such as increased voiding and solderability issues which immensely effect the lifetime and reliability were investigated intensively in the last decade [55; 56; 57; 58; 59; 60; 61; 62]. In general, the reflow solder process provides a high yield, high reliability, and low cost advantages when performed properly. Among all of the process considerations, reflow profile is one of the most important factors in determining soldering defect rate. The types of defects affected by reflow profile

include component cracking, tombstoning, wicking, solder balling, bridging, solder beading, cold joints, excessive intermetallics formation, poor wetting, voiding, skewing, charring, delamination, leaching, dewetting, solder or pad detachment, etc. Therefore, it is extremely important to have the reflow profile engineered properly in order to achieve both high yield and high reliability.

In case of high-temperature electronics especially power electronics, voiding is one of the main problems and has been researched intensively to understand the influence on the lifetime and reliability [63; 64; 65; 66]. A low and homogeneous thermal resistance of solder joints is demanded for a quick and uniform conduction of the heat loss from the components. The same applies for the electrical conductivity of solder joints. Enclosed voids can cause a displacement of electrical and thermal paths and a local concentration of power and heat. In addition, gas voids are prone to form spheres in the solder gap, which could be a cause for tilting of components and a wedge-shaped solder gap particularly in large-area interconnects. This escalates the problem of non-uniform current or heat distribution and causes stress and cracks in the joint. According to the the norm DIN EN 61191-6 [67], the voids are classified into three types namely voids inside the solder (Type C), voids near to component surface (Type D), voids near to the substrate (Type E). These can be further illustrated into the types of voids as in Figure 15 in the perspective of power electronics bare dies. The voids inside the solder might increase the solder height or eventually tilt the component. The voids near to the component or substrate side and the micro-pores observed at the IMP borders at the substrate surface in Cu3Sn layer might initiate or support crack formation. This is not just limited to the die-attach on the DCB but also DCB soldering to the baseplate in case of multichip power modules.

Though in case of large-area joints, the effect of small voids is negligible, but a tilt of the soldered DCB due to Type C void formation brings uneven distribution and leads to delamination or crack formation affecting the components above further. The amount of voids can be influenced by different measures, e.g. a good wettability of metallization, solder pastes with special adopted solvents and an adequate preheating profile.

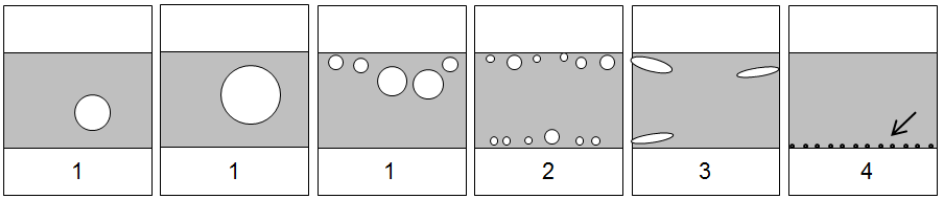


Figure 15: Types of voids generally observed in electronic assemblies [57].

2.3.2 Packaging and Module Concepts Requirements

The evolution of power semiconductors has arrived at a level where packaging restricts the achievable performance of the final device. This statement already holds for today´s silicon technology and will get worse for WBG integrated electronics with ultra-fast switching and high power densities. A package for a power semiconductor has to remove the heat, provide secure insulation against the heat sink, conduct current and has to be electro-magnetically and thermo-mechanically reliable. The development of solutions for these multiple requirements has to be based on in-depth knowledge of application demands as well as material and production processes.

As summarized from the roadmap and survey analysis in above sub-chapter, the developments in power electronics packaging have to face the following aspects:

- increase of power density requires more sophisticated thermal design
- the possibility for higher junction temperatures can only partly be used due to the negative impact on reliability. But allowing a higher operation temperature would reduce system volume due to smaller heat sinks
- more functions in the package or module can reduce system costs
- cost efficient production processes always remain an issue for improvements

A very good thermal conductivity is necessary at all materials in the construction of time to discharge the losses in form of heat from the power components as quickly as possible. Irrespective of the type of the packaging technology, to ensure the semiconductor reliability, the modules are designed for uniform heat dissipation from the components. The thermal resistance (R_{th}) is an excellent characterization factor for power modules and achievable current densities. The packaging technologies i.e. materials must have low thermal resistance in whole package. To achieve this, the thermal resistance is reduced by either using active cooling techniques

directly at the substrate or baseplate level. For the compound layers made of solder, this results in the requirement of a possible void-free and uniform solder joint in thickness and area. This brings a significant difference in the performance characteristics when the silicon is replaced by the new generation WBG materials. Increased enclosed gas bubbles or particulates selectively increase the thermal resistance and thus lead to unwanted hotspots. An uneven solder gap also prevents a uniform thermal conductivity (λ_{th}) over the entire structure in the path to cooling device [68]. Both thermal and thermo-mechanical behaviors of the structure have a significant impact on its long-term reliability. Different coefficients of thermal expansion (CTE) of the materials used lead to stresses in the material that degrade in the case of the solder layers due to creep. Resulting microcracks in turn lead to increased local heating and speed up the thermo-mechanically induced aging process to failure by delamination at the interconnection layer.

The main reason is the creep relaxation process and thus the aging behavior of the solder joint which is dependent on temperature. Reinforced creep behavior occurs in alloys with a homologous temperature of $T_H \geq 0.4$ [69]. The homologous temperature thus serves as a guide to what thermal load to connect without accelerated aging and reliable operation. It is defined as:

$$T_{HX} = \frac{T_{XOperation}\,[K]}{T_{Liquidus}\,[K]} \qquad [1]$$

A SnAgCu solder joint ($T_{Liquidus}$ ~ 220 °C) has a homologous temperature of T_{H150} of 0.86 and T_{H200} of 0.96. Generally for a $T_{HX} < 0.5$, the operation is considered to be stable [69]. For operating temperatures ≥150 °C is therefore expected a significantly accelerated degradation in the solder joint. The service life with thermo-mechanical loading thus decreases enormously [57]. The WBG materials such as GaN or SiC allow operation of the power semiconductors at temperatures above 200 °C, which evidently shows that the soft solder based interconnections are to be absolutely replaced. In the field of materials, there are presently several development trends for interlayers with high melting metals like Ag and Cu. The silver based interconnec-tions depending on the porosity have T_{H200} to less than 0.4. The combinations of Cu with Sn i.e. with increased Cu content increases the T_{H200} to less than 0.6. The silver sintering and diffusion soldering are two important alternatives with potential to be integrated for high-temperature operation which are explained in next sub-chapter 2.4 in detail.

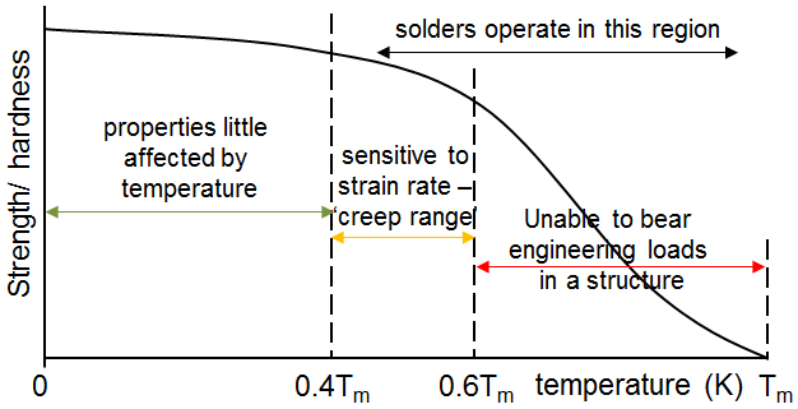


Figure 16: Strength of a material related to its melting temperature; modified from [69].

2.4 State-of-the-art High-temperature Interconnects

In order to take advantage of excellent electrical properties of SiC and GaN devices, an assembly process is required, which allows the high-temperature operation of the produced module without any deterioration of electrical characteristics. Currently for high-power applications and high-temperature operation upto minimum of 400 °C, the set of assembly processes and materials are limited and assembly technology is yet not fully mature. The major challenges are mechanical, thermal and electrical stability of packaging materials [70]. For instance, the current state-of-the-art high-temperature die-attachments such as AuSn and AuGe solders melt at 280 °C and 356 °C respectively, which limits their operational capability well below their melting points (T_{H200} of 0.86 and 0.75 respectively). These materials are costly and lead to increase of overall costs due to high processing temperatures for production. The high-temperature stability, matching of CTE between different materials, and other material properties such as thermal conductivity, electrical conductivity and elastic modulus etc. become very critical for these materials. The commonly available top-level interconnection materials such as Cu, Al etc. undergo oxidation at temperature greater than 200 °C [70]. The extreme thermal cycling conditions during operation can cause high thermal and thermo-mechanical stresses on the package, which significantly reduces the package lifetime. All these factors open a broad scope for research on high-temperature stable assembly materials and processes.

The high-temperature stable die-attachment (i.e. chip to substrate) needs to stable up to minimum of 400 °C [70] to be stable against the temperature fluctuations to avoid power discrepancies [46]. The thermal conductivity of

the die-attach material must be high to dissipate the heat generated in the active area of the device during high-power operation [71]. This holds true for both lateral and vertical designs of the semiconductor devices. For power devices with vertical design, the electrical conductivity of the die-attachment material should be high to achieve high-power levels [72]. The CTE of chip, die-attach and substrate must be matched in order to minimize the thermo-mechanical stresses, which are produced during the die-attachment process and also during the high-temperature operation of the semiconductor devices [15].

2.4.1 Silver Sintering

As mentioned previously, there are presently two main techniques to achieve stable high-temperature die-attach interconnections. These are the low-temperature silver sintering and diffusion soldering where the former being presently dominating in the industry [18; 73]. Both the techniques are pressure-assisted to achieve the optimal bond quality. The pressure-assisted low-temperature sintering for the electronic devices was first demonstrated by bonding large area silicon chips on top of the molybdenum substrates [74]. The used Ag-powders and flakes were covered with organic additives to protect them from agglomeration and aggregation at room temperature. These help also in the printability of the pastes onto the substrate materials. Other organic binders and sinter additives are often included in the silver paste containing these micron-sized flakes and particles. The organic additives burn out at temperatures between 180 °C and 200 °C [75]. Here oxygen is often required to remove theses organic additives around the silver particles and flakes. The technique is based on the atomic diffusion of silver into the bonding surface generally with similar surface finish on the diffusion barrier layers like nickel [74]. The external pressure helps to reduce the sintering temperatures in the range of 225 °C to 300 °C. The pressure assisted Ag-sintering process is carried out in the following steps [76; 17; 77; 78; 79].

1. Application of Ag-sinter paste using screen printing in thin layers on the substrates generally between 60 - 80 µm.
2. Drying of the paste at 150 °C to burn out the organics in the paste.
3. Placement of the electronic component on the dried paste.
4. Sintering of the component is performed at temperature range of 225 °C to 300 °C using pressure-assisted sintering process i.e. 10 MPa to 40 MPa. The sintering is carried in atmospheric air or in nitrogen environment.

A lot of research was performed to understand the approach with respect to the process influential factors as pressure, temperature, particle size and shape, etc. [80; 81; 82; 83]. The main quality factor here is the porosity of the produced sinter joint which significantly decides the mechanical, electrical and thermal properties. This is enhanced by the application of external pressure in range of 30 - 40 MPa [80].

The particle size of the silver reduces the process temperature by increasing the surface energy during bonding process. However the applied pressure must be uniform where the surface properties like planarity and roughness of the components are of very high importance. The aggregation of the silver particles is also an important factor during the bonding process. Due to non-uniform paste application or improper drying of the solvents, the particles form a strong chemical bond leading to large voids in the sinter joints. The applied pressure and planarity are very critical as they can lead easy breakage or cracking of components mainly brittle Si materials on the substrates. The literature describes a number of key advantages of the Ag-sintered layers, which are based on sintering pastes, formed using both nanoscale and microscale particles [80; 76; 81; 80; 84].

- The melting point of Ag-sintered layer depending on the porosity is around 960 °C, which is four times higher than the bonding temperatures.
- The homologous temperatures are $T_{H200} = 0.38$, $T_{H400} = 0.55$ respectively show clearly the capability of high-temperature operation.
- High thermal conductivities up to 200 W/mK depending on the achieved joint porosity and the electrical resistivity is very low i.e. ~3.6 × 10-6 Ωm.
- Very thin die-attach thicknesses i.e. 30 µm or less can be achieved with very low thermal resistance reducing the overall package thermal resistance.
- Excellent reliability during passive thermal and active power cycling compared to soldering or other medium-temperature interconnects.

However, there are notable disadvantages of the Ag-sintering mainly

- The process time compared to soldering is relatively long (minutes to hours).
- The pressure-less sintered layers contain large porosities and often displays significantly low mechanical stability (even with longer process times).

- The application of high mechanical pressure brings breakage or micro-crack formation in the chip during the pressure-assisted sintering.
- The material properties of the Ag-sintered layers are largely dependent on the process conditions i.e. sintering pressure, sintering temperature etc.
- This technique is limited to very few designs for high reliability due to process complexity and quality control.
- The bonding material and the equipment costs are very high compared to the conventional soldering techniques.

2.4.2 Diffusion Soldering

Diffusion soldering is the enhanced variant and hybrid concept of diffusion bonding and conventional soldering technology based on the principle of the isothermal solidification and transformation into IMPs [19; 85]. A detailed description of diffusion soldering, influential parameters and variants are given in the following chapter. This technique is useful for high-temperature bonding only if the IMPs are formed in the complete bondline. Here the bonding process parameters mainly process temperature and time should be reasonable to be implemented into serial or mass production. Presently, in few power electronic and micro-electronics applications, pressure-assisted diffusion soldering is carried out [86; 87; 85]. Similar to Ag-sintering, the mechanical strength and durability is prolonged compared to soft-solders, but is also limited to very few designs because of the involved process complexity and equipment costs. For initializing a diffusion process, the metal systems have to be homogenously mixed followed by appropriate thermal energy input. Though the above pressure-assisted Ag-sintering and pressure-assisted diffusion soldering is limited to very specific models, the pressure-less diffusion soldering process if realized, could be an efficient and customizable alternative for conventional soldering and Ag-sintering in the future for reliable power modules. Table 2 gives an overview of the researched metal systems and the expected intermetallics with their melting points. The bimetallic systems of gold and silver as HMMs and tin and indium as LMMs as contents of the interlayer material between the parent HMM components or supporting metallizations are being researched. Still the cost of the assemblies could not be reduced due to the rare metals as HMM contents. Copper as HMM was considered as a cost-effective alternative with combination of tin or indium as LMMs. In case of Cu-Sn interconnect systems where Cu_6Sn_5 and Cu_3Sn are produced.

Table 2: Overview of the formed IMP for various metal interconnect systems

Interconnect materials	Intermetallic phases	Melting point (°C)	Elastic modulus (GPa)
Au-Sn	Au_5Sn, $AuSn_2$	> 278	76 - 88
Au-In	AuIn, $AuIn_2$	> 495	78 - 87
Cu-In	CuIn, $Cu_{11}In_9$	> 307	109 - 139
Ag-Sn	Ag, ε (Ag_3Sn), ζ ($Ag_{85}Sn_{15}$)	> 600	78
Ag-In	Ag, Ag_2In, Ag_3In	> 880	89 - 124
Cu-Sn	Cu_6Sn_5, Cu_3Sn	> 415	112 - 134
Cu-Sn-Ni	Ni_3Sn_4	> 796	133

Advantages and disadvantages of TLP/ IMP formation

An overview of the material properties of the interconnect systems and the formed intermetallics in different material systems are given in Table 3 [88; 89; 90; 51; 91; 92; 93; 94; 95]. The following advantages are outlined compared to other assembly techniques [96; 97; 98; 99].

- The obtained bondline has higher remelting temperatures and can operate at much higher temperatures than the bonding temperature.
- Due to the microstructural behavior, the material properties mimic the properties of the base metal. In some cases, the bonded area becomes indistinguishable from the other grain boundaries due to significant diffusion. Such bonds are often as strong as the bulk substrate materials [96; 97]. But this does not occur in thin-film based interlayer systems.
- The surface requires less preparation before bonding process. No fluxing agent is required, however treatment with reducing agents in case of oxide-prone metals is needed.
- The liquid formed at the interface during TLP process fills the unevenness of the mating surfaces and makes the costly surface finishing processes unnecessary [38].

The main disadvantages of TLP bonding are as follows:

- The process is expensive compared to the other die-attachment processes.

- The formation of thicker layers of intermetallic compounds in the TLP joint may cause to lower its strength and ductility.
- The time required for the isothermal solidification and sufficient bond homogenization can be unfeasibly long.
- Formation of interlayer metal oxides may hinder the process [59].

Table 3: Electrical and mechanical properties of the interconnect systems

Interconnect systems		**Melting point (°C)**	**Elastic modulus (GPa)**	**Thermal conductivity (W/mK)**	**CTE10^{-6} (ppm/K)**	**Electrical conductivity x 10^5 (Ωcm)$^{-1}$**
Lead based solders	$Sn_{63}Pb_{37}$	183	30.2	50.9	21 - 24	0.6
Lead-free soft solders	$Sn_{96.5}Ag_{3.5}$	221	50 - 56	78	22.2	0.8 - 1
	$SnAg_{3.0}Cu_{0.5}$	217/220	50	63.2	21	0.8
	$Sn_{99.3}Cu_{0.7}$	227	64.6	65	22	0.6 - 1
High-temperature solders	$Au_{80}Sn_{20}$	280	68	57	16	0.63
	$Au_{88}Ge_{12}$	356	74	44	12	-
Silver sintering	Ag (flake)	961	9 - 60	100 -240	18 - 23	2.6 - 3.9
Diffusion soldering	Cu-Sn system	> 415	> 80	70.4	16.3 - 19	-

The above disadvantages are focused in this thesis work to optimize the bonding parameters, intermediate IMP formation and the implementation into large-scale production. Table 4 gives an overview of the IMP formed in the copper, tin and nickel combinations of the interlayer. For the copper and tin combination, the intermetallics of Cu_6Sn_5 (η- phase) and Cu_3Sn (ε-phase) are formed depending on the bonding temperatures. Compared to pure tin which is generally the final part of the bondline, the mechanical, thermal and electrical properties of the IMPs are relatively high. Though the formation of these IMPs is considered as disadvantage in electronics production due to crack formations generated by the CTE mismatch, a full IMP formation in the bondline could significantly improve the performance of the complete interconnection. However a full transformation of the joint into ε-phase is associated with longer process times or pressure assistance which is not the focus of the thesis. The main aim lies in the

formation of η-phase i.e. Cu_6Sn_5 in the complete bondline to achieve the above mentioned properties.

Table 4: Room temperature physical and thermal properties of intermetallics [100]

Property	Cu	Sn	Ni	Cu_6Sn_5	Cu_3Sn	Ni_3Sn_4
Density [g/cm³]	8.9	7.3	8.9	8.28	8.9	8.65
Young's modulus [GPa]	117	41	213	85.56	108.3	133.3
Vickers hardness [kg/mm²]	30	100	15	378	343	365
Electrical conductivity x 10^5 $(\Omega cm)^{-1}$	5.8	0.8	1.2	1.1	5.7	0.35
Thermal conductivity [W/(m.K)]	3.98	0.67	0.90	34.1	70.4	19.6
Thermal diffusivity [cm²/s]	-	-	-	0.145	0.24	0.083
Specific heat [J/(g.K)]	0.385	0.227	0.439	0.286	0.326	0.272
CTE x 10^{-6} [K^{-1}]	17.1	23	12.9	16.3	19.0	13.7

Table 5 gives an overview of the process conditions for various interconnection technologies including conventional soldering, Ag-sintering and diffusion soldering of various material combinations. It can be observed that various process conditions mainly the time and temperature were varied to achieve the intended interconnections and properties. From the references, it can be inferred that the process parameters were intensively investigated for the material systems and the requirements for the quality in the intended application. In case of diffusion soldering, the process temperatures however are basically defined by the melting point of the LMM component i.e. in the range of 180 - 200 °C for indium and 250 - 280 °C for tin based combinations. The Ag-Sn TLP requires either low mechanical pressure with short process time or pressure-less bonding for 60 min. In case of Cu-Sn systems, the process conditions of at least 280 °C with pressure assistance is required to achieve in short process times. For Ni based combinations, the process temperatures also go to above 250 °C to form intermetallics of Ni_3Sn_4 similar to Cu-Sn system. The process conditions are similar to pressure-assisted silver sintering.

Table 5: An overview of the die-attachment process conditions

Type of inter-layer materials	Process temperature [°C]	Process time [min]	Conditions (pressure, process gas)	References
$Sn_{96.5}$ $Ag_{3.5}$	250	1 - 1.5	Air	-
Au80Sn20	320	0.5 - 4	N2, Ar	[101]
Au-Sn TLP	260	15		[102]
Au-In TLP	200	0.5	Vacuum	[103]
	160-240	1-10	10 - 30N	[102]
Cu-Sn TLP	280	4	6 MPa	[102]
Cu-In TLP	180	4		[102]
Ag-Sn TLP	250	60	-	[103]
	260	10	1.2 N/100 N, N_2	[104]
Ag-In TLP	210	10	0.3 MPa, N_2	[105]
	175	120	Vacuum	[99]
Ag-sintering (Nanoscale)	150	30 - 60	No pressure, Air	[106]
	280 -350	15 - 60	No pressure, Air/ N_2	[107]
Ag-sintering (Microscale)	225-275	3 - 15	5 - 40 MPa, Air/ N_2	[108]

2.4.3 Top-level Interconnections

The current dominating standard for frontside connections is aluminum-based ultrasonic thick-wire wedge bonding or ribbon bonding for power devices. The lifetime is not only limited by the bond interface but also by the wire material. This is also related to the quality of the back-side interconnection i.e. die-attach, where a defect can substantially increase the junction temperatures and eventually trigger bond wire degradation or crack formation in the wire or the bond interface. The wire bonds for high-temperature operation also should be capable of withstanding temperatures as high as 400 °C. Here various issues arise with increased temperatures as oxidation or reaction with mold or encapsulation materials.

The mechanical stability and current densities or current carrying capability of the material i.e. electrical properties should not vary with temperature. [70; 109; 110; 111; 112; 48; 113].

An advancement for the increased lifetime is usage of copper material replacing aluminum. Due to the process complexities for copper wire bonding, semiconductors should be copper metallized and the bonding parameters must also be optimized. The implementation of the copper wire bonding process into mass production needs significant changes with bonding and cutting tools due to better mechanical characteristics of copper compared to aluminum [114; 115; 116]. But wire bonding with thick copper wires also needs new metallization systems on semiconductors that are still to be optimized and made compatible with the following packaging steps. This thick copper frontside metallization also brings process defects like warpage and solder displacement during soldering process, making the assembly unfit for further wire-bonding process. Other alternatives presently in research are the Al-cladded copper wire bonding and SKiN Technology [30; 117]. A reliability of 20-time higher cycle strength with regard to load changes was obtained by using Aluminum-cladded copper wire-bonds and Ag-sintered assemblies compared to semiconductors with aluminum wires [118]. To avoid completely the weakness in the module, few designs without wires are opted with double sided soldering or sintering as explained in the sub-chapter 2.1. [32; 119]

Rapid prototyping through additive metallization is also an important development in times in which fast and flexible manufacturing processes are required. Other drivers for rapid manufacturing are resource restrictions and high demand for energy efficient processes. The development of functional layer materials also benefits this technology. Very relevant are e.g. layers that have a high conductance on ceramic materials. As the metallization quality of the layer- materials and processes is reproducible the application of additive metallization could also be interesting in mass production. This also supports the future trends of 3D-power electronics through integration of various additive manufacturing technologies for ceramic substrate technologies and high-temperature embedding concepts with new generation WBG materials.

3 Diffusion Soldering as High-temperature Interconnect

For the high temperature modules and integration of new generation WBG semiconductors, as mentioned above, silver sintering dominates the industry as high-temperature interconnect next to the gold-based eutectic solder materials. The diffusion soldering technology is an alternative which has the potential for serial or even mass production with high level of customization and flexibility. The basic idea in diffusion soldering as introduced in previous chapters is to transform the interlayer with LMM and HMM contents into IMPs. The produced IMPs have a higher remelting temperature than the used interconnect material or the processing temperatures [19; 86; 96]. Depending on how the interconnect materials are made available for connecting the components, the diffusion soldering can be basically divided into Transient liquid phase bonding (TLPB) and Transient liquid phase soldering (TLPS).

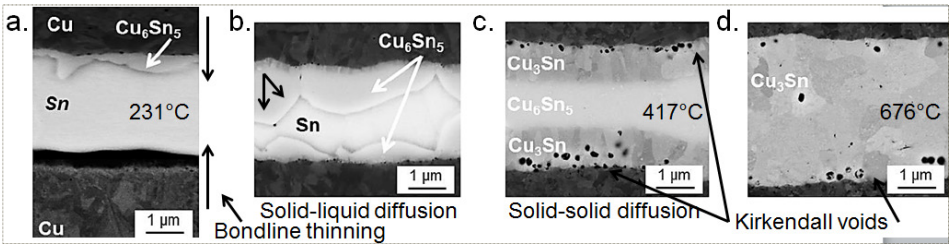


Figure 17: Overview of TLPB/ SLID bonding with solid-liquid and solid-solid diffusion in a Cu-Sn system for fine pitch applications in microelectronics [86].

The TLPB technique also known as solid-liquid interdiffusion (SLID) bonding finds application in fine-pitch micro-electronic applications in 2.5D/ 3D-wafer level packaging (WLP) mainly chip-to-chip or chip-to-interposer connections. In Cu-Sn SLID bonding, the Cu and Sn thicknesses are generally from 3 to 10 µm and ~5 µm respectively [86].The applicability of this technique is limited to SLID contacts and partially for Cu-pillar interconnects up to 50 µm with full Cu_3Sn transformation or combination of Cu_3Sn and Cu_6Sn_5. The interconnect materials are usually made available in thin layers based on thin-film deposition techniques such as sputtering and e-beam evaporation, where layers of Cu, Sn or Ag are deposited as chip backside metallization. For interconnect heights above 50 µm e.g. flip-chip contacts or Wafer-level chip-scale packaging (WLCSP) to BGA interconnections ranging to 800 µm, the applicability of TLPB is untouched due to

process-related complexities. To fully wield the advantages of these highly remelting IMPs systems as a high-temperature alternative for large-area interconnects, the IMPs must be produced in the complete bondline between the parent HMM components. The TLPS technique where the interconnect material is made available in form of pastes or preforms with abundance of copper for IMP formation can be an approach for large-area interconnects as in power electronics. As part of this work, the paste- and preform-based TLPS techniques are investigated.

3.1 Mechanism and Process Flow

Irrespective of the type of metal combinations implemented, the mechanism observed in this technique is the atomic-level diffusion. It is the diffusion process whereby the random thermally-activated movement of atoms results in the net transport of atoms. It can be defined as the mass flow process in which atoms change their positions relative to neighbors in a given phase under the influence of energy gradient i.e. thermal or mechanical. Diffusion can occur mainly by two mechanisms namely interstitial or substitutional diffusion [120]. Substitutional diffusion occurs by the movement of atoms from one atomic site to another. For the swapping of atoms, it takes large amount of energy to physically push the atom out of its home lattice. This generally happens only if a vacancy is present. In case of interstitial diffusion, diffusing atom is free to move to any adjacent interstice, unless it is already occupied. Generally substitutional type is slow compared to the interstitial diffusion. Many factors influence the diffusion process where the diffusing species is one of them. If the diffusing species is able to occupy interstitial sites, then it can easily diffuse through the parent matrix. On the other hand if the size of substitutional species is almost equal to that of parent atomic size, substitutional diffusion would be easier. Thus size of diffusing species will have great influence on diffusivity of the system. In case of bimetallic systems like copper and tin, the substitutional diffusion is easier as the atomic size of Cu is less than Sn. This forms the basis of the diffusion soldering process.

In this thesis mainly the Cu-Sn systems are investigated. In case of solid Sn, upon thermal excitation Cu atoms are able to move easily because of rapid, small-amplitude vibrations about their equilibrium positions. Such vibrations increase with temperature and at any temperature, a very small fraction of atoms has sufficient amplitude to move from one atomic position to an adjacent one. The fraction of atoms possessing this amplitude

increases with rising temperature. In jumping from one equilibrium position to another, an atom passes through a higher energy state since atomic bonds are distorted and broken.

Temperature has a most profound influence on the diffusivity and diffusion rates. It is known that there is a barrier to diffusion created by neighboring atoms that needs to be distorted to let the diffusing atom pass through. Thus, atomic vibrations are created by temperature assist the diffusion of the migrating species. Diffusion is faster in open lattices or in open directions than in closed directions. The defects like dislocations, grain boundaries act as short-circuit paths for diffusing species, where the activation energy is less. Thus the presence of defects enhances the diffusivity of diffusing species. When the low melting material is heated, the broken bonds or the fluidic matrix helps in increased diffusivity of high-melting free Cu atoms. This also explains the increase of Cu concentration in Sn material upon thermal activation than vice versa [121; 122].

But over the time two more phases form due to diffusion phenomena. It is commonly known that Cu and Sn reacts with each other at the interface to form intermetallic compound of Cu_6Sn_5 and Cu_3Sn. The intermetallic Cu_6Sn_5 forms faster due to low activation energy and grows with scallop-like morphology as Cu atoms diffuse inside Sn through fast atomic transport phenomena.

In the early stages of the diffusion process, Cu atoms dissolve into the molten Sn and form Cu_6Sn_5 IMPs at the low temperatures as Cu atoms diffuse faster in Sn. Further Cu_6Sn_5 reacts with Cu and forms Cu_3Sn IMP. [50] The reaction kinetics are given below which also explains the micro-void formation at the Cu/Cu_3Sn interface due to Cu consumption:

$$6\ Cu + 5\ Sn \rightarrow Cu_6Sn_5$$

$$Cu_6Sn_5 + 9\ Cu \rightarrow Cu_3Sn$$

Process flow for diffusion soldered interconnects

Diffusion soldering describes a bonding technique based on a metal interlayer, which is melted and solid-liquid as well as solid-solid diffusion in the interlayer material is stimulated. This is also the main difference to common diffusion bonding where only solid-state diffusion occurs. As in this thesis work, the focus lies in Cu-Sn system in power electronic applications, the sequence of steps is explained in power packaging perspective. The mechanism of diffusion process can be divided into the following steps as in Figure 18 and explained as follows:

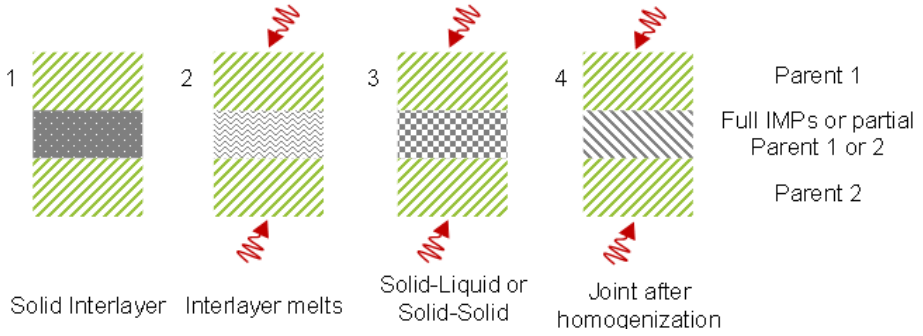


Figure 18: Schematic illustration of the sequence of steps for diffusion soldering.

1. Setting up the bond with printed or placed interlayer materials and components
2. Heating to the specified bonding temperature to liquefy the low-melting layer in the bond region i.e. greater than the melting point of interlayer Sn
3. Holding the assembly at the bonding temperature until the liquid has isothermally solidified due to interdiffusion
4. Homogenizing the bond at a suitable post handling temperature

Setting up the bond

The joining material generally Sn compatible for low-temperature bonding processes is procured in form of metallization or thin foils or pastes between the two parent metals with high melting points. The higher melting component is the substrate material (e.g. copper from substrate) or can also be in form of metallizations of parent materials (copper as chip backside metallization). The interlayer and parent materials remain solid at this point since no there is no energy input or thermal activation.

Solid-state diffusion

The first diffusion begins right when the assembly is initially heated. Depending on interdiffusion coefficients of interlayer and parent material as well as the temperature-gradients, a certain amount of low melting material diffuses into the substrate. This generally is also the starting point for IMP formation observed in electronic assemblies, where the IMPs like Cu_6Sn_5 and Cu_3Sn form at the interface.

Melting of the interlayer

Before the melting temperature of the interlayer is reached, the materials in few cases are treated with reducing agents to remove the oxide formation and contamination to obtain low-defect bonds. The liquefaction of the

bonding material begins enabling the liquid layer to fill the voids formed by surface roughness of the joining surfaces. It may also dissolve any residual surface contaminations at the interface and eventually wets the complete surface. The set-up is then further heated up to the specific bonding temperature to ensure the complete melting of the interlayer metals and for further diffusion.

Dissolution of the substrate material

While reaching the bonding temperature, the liquid material follows the liquidus and solidus lines of the phase diagram, illustrated by the liquidus and solidus concentrations. In order to conserve its mass, some part of the adjacent parent material is dissolved. The concentration of substrate material in the melting zone rises. An expansion of the liquid region can be observed at that point. This process continues until the liquid concentration reaches its maximum at the bonding temperature. With time, the liquid layer at the interface diffuses into the parent metal which results in isothermal solidification and narrowing. At this point, if desired the bonding process can be stopped. The bond already has an elevated remelting temperature as compared to the melting temperature of the interlayer metal (i.e. Cu_6Sn_5 in case of Cu-Sn systems). There could be some remaining interlayer material depending on when the process is stopped.

Isothermal Solidification

Further treatment at the bonding temperature continues the solidification process. At this point a maximum in melt volume is detected due to the previous dissolution reactions. Now, the diffusion reactions work in the opposite direction: Interlayer molecules are drawn in the substrate, accelerating the formation of intermetallic compounds on the solid-liquid interface. This leads to a contraction of the bonding zone. Finally the whole liquid is consumed, leading to a concentration profile. This phenomenon is called isothermal solidification. Here due to the usage of the low-melting material, micro-voids or interfacial lateral voids are observed in the bond line due to the already formed solid structures. Without an external support like mechanical pressure, the defects might increase exponentially over the complete bonded surface. The interfacial bonds also increase if two high melting materials with a CTE mismatch are bonded together.

Homogenization

Normally, the bonding process is not over at that point. The following steps focus on the further reduction of pure interlayer material, meaning the generation of more intermetallic phases at the expense of the residual

initial interlayer material and therefore a rise in melting temperature of the compound. These measures can be done in the normal processing furnaces or in a different heat treating apparatus at a different time (Cu_3Sn in case of Cu-Sn systems).

An overview of the process parameters is also given in the following Table 6. It can be observed that the surrounding conditions play a major role in the profiling of the process for acceleration of the IMP formation. It is relatively difficult to achieve fully- IMP transformed defect-free bonds without mechanical pressure where the important process step of isothermal solidification takes hours. These defects increase exponentially with the interlayer height or the diffusion distances. Even though the heat treatment leads to a higher melting point and reliability due to the higher concentration of IMCs, practically equilibrium has to be found between economical and technical requirements.

Table 6: Overview of the process time and surrounding condition, process variables of TLP bonding [123; 96; 124; 125].

Process step	Process time	Surrounding condition
Heating to bonding temperature	Less than a minute to about an hour	Moderate pressure
Melting of interlayer	Less than a second to several seconds	Moderate pressure
Melting back of parent metal	Seconds to minutes	With mech. pressure
Isothermal solidification	Seconds to minutes/ minutes to hours	With mech. Pressure/ without mech. Pressure
Homogenization	Hours to days	No mech. pressure

3.2 Production Methodologies

The basic principle of diffusion soldering now called as TLPB/ SLID technology was presented by Bernstein in 1966 for the first time [87]. This was then further demonstrated for micro fine-pitch contacts in micro-electronics and large-area contacts for power semiconductors as well [85; 103]. The production methodologies were largely focused on the hermetic packaging or microelectronic applications, but not specifically on the scaling for the large-area interconnections. The main reasons were the complexities and quality control in the process. These are further discussed in following sub-sections. The reaction kinetics of the IMPs are mainly dependent on the parameters as follows:

1. Temperature (pre-heating, peak, post-handling)
2. Time (peak and post-handling) and thermal gradients
3. Interconnect material composition (filler metals and base flux materials)
4. Surrounding conditions mainly pressure and process gases

The time frame of the TLP bonding is highly dependent on the material system and the experimental parameters such as bonding pressure, temperature, interlayer thickness etc. The duration of the bonding for individual stages of the TLP bonding described in Table 6. The heating of the assembly and the homogenization is carried out with ovens equipped with various energy transfer methods mainly heating such as radiation, conduction, or induction generally carried out under vacuum [96; 125; 126]. However, the process gases such as nitrogen [96; 104], hydrogen [105], and forming gas [123; 127] are also being used. External pressure is usually applied to the assembly mainly to accelerate the IMP formation and for the alignment of the assembly components. Mechanical pressures between 0.1 and 10 MPa are used [96; 128; 124] based on the sensitivity of the components and application i.e. fine-pitch or large-area contacts.

3.2.1 State-of-the-art TLPB and TLPS Approaches

Immense research had been conducted in the feasibility of the combinations of multi-metal systems and characterization of the produced IMPs. But little research has been focused on the scalability of the technology for mass production, where the TLPB is limited to prototype development or low-scale production. This holds true for both the applications of fine-pitch micro-electronic or large-area power electronics. Figure 19 gives an overview of the state-of-the-art production methodologies for TLPB and TLPS. As explained earlier, Berstein introduced this technique for electronic applications with interlayer material as tin or indium [87]. To allow a short processing time, the film thickness of the interlayer was usually less than 10 µm and could be applied both electrically and by vapor deposition. Major application stays with the fine-pitch contacts for 3D-intergration at wafer level, where very high surface quality and component or joining accuracy is required. [85; 86] This was one of the main drawbacks, where the high roughness of the power electronic substrates hinders the applicability. Upon series of experiments had led to successful application of the process specifically with approaches as in Figure 19.a, b to typical power semiconductors with an area of around 100 mm^2. The company Infineon Technol-

ogies AG sold the OptiMOSTMT2 named power devices with this technology [129; 73]. The main requirement here was the bonding force required to shorten the process time and to ensure full IMP transformation. The diffusion rates in case of Ag-Sn are faster compared to Cu-Sn, but due to cost factors, the focus was shifted mainly with focus on scaling the technology for power electronics using Cu-Sn systems in the projects of HotPowCon and ProPower. Mainly next to the TLPB approaches, especially for TLPS, the topology approach, composite solders approach, thin-layer solder approach were investigated [130; 131; 132; 133; 134].

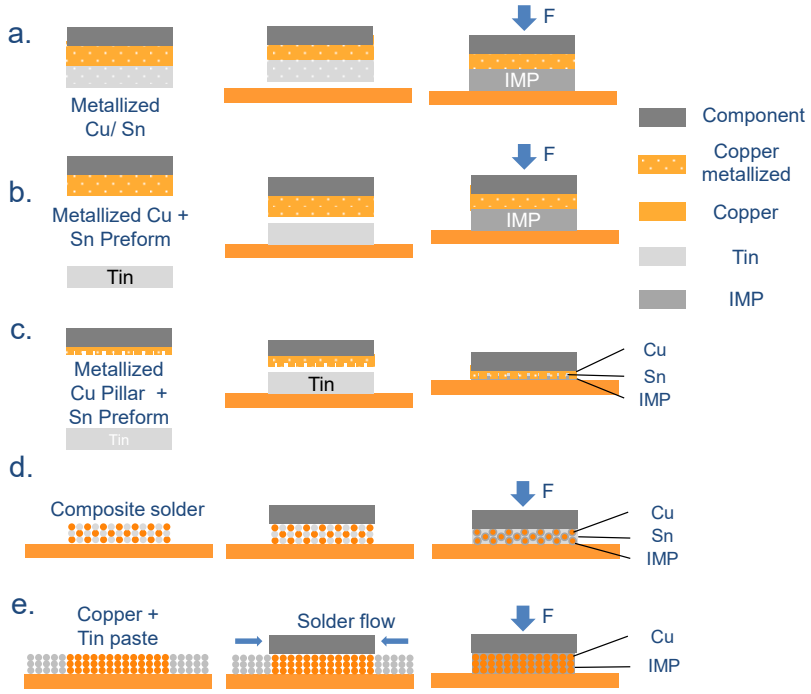


Figure 19: Various approaches followed in case of TLPB (a, b) and TLPS (c. topology, d. composite solder, e. lateral flow approach)

Topology Approach: Another variant namely 'Topology approach' was realized in project 'HotPowCon' where the chip base-side metallization was modified with pillar structures as in Figure 19.c. Here the interlayer under the pillar transforms into IMP with local distribution of partial IMP structures over the complete bondline. Here bonding force was not required which enables the partial-TLPS with conventional reflow soldering. But the presence of rest tin from the interlayer however is considered as a defect prone region where the full advantages of the TLPS are not realized. [130;

134]. The topology or design requirements are still under investigated and are not fully optimized for full-fledged IMP formation.

Composite Solder Approach: Further investigation followed by the modification of the interlayer materials with composite materials to reinforce the IMP microstructure. A composite solder is a mixture of powder filler materials to base composition to improve the material properties of the interlayer materials. Here the fillers can be micro- to nano-sized particles [135] of metals, intermetallic phases [136] or even ceramics [137]. An overview was given by GUO et al. [138].

For the TLPS using composite solders, the fillers should have a higher melting temperature than the solder alloy (i.e. Cu in case of Cu-Sn TLPS as in Figure 19.d). During the bonding process, the filler reacts with the solder material to form IMPs. To achieve this, a powder mixture of solder and filler material is processed into a paste which is then applied and soldered. The particles turn into a cluster of IMPs with filler particles between the two joining partners. The diffusion distances in such case are reduced greatly ensuring full IMP formation. In case of composite solders, sufficient mechanical strengths of the compounds has already been demonstrated for high temperatures with copper filler content up to 60% [139; 140; 141]. A complication of this approach is the high void content in the bondline compounds, which increases with an increasing proportion of the high-melting component in the paste [132]. This is due to the formation of network of copper particles and deficit of low melting material, where a skeleton or scaffolding structure can be observed. In order to reduce the high pore content caused by the scaffolding, further investigations were performed to optimize the process.

In the enhanced process, the composite solder containing no-flux was applied to the substrate and then the chip was assembled and soldered under a high bonding pressure. Here some solder material is forced out of the solder gap during soldering due to the non-wetting of solder to the copper particles. In a second process step, the interconnection is exposed and remelted in formic acid environment. Only by activating with formic acid, the solder can wet out the copper particles and the partners. Thus, the previously squeezed out solder is again drawn into the solder gap enabling a pore-free connection [132; 141]. The process has been demonstrated, however it has been not yet proven possible to produce a virtually pore-free connection.

A similar technology is the 'Ormet technology', where a paste of epoxy resin, copper powder and tin-bismuth solder powder was used. Though

here conventional soldering processes could be used, the obtained interconnections showed temperature resistance of 400 °C but with very high epoxy-filled pores [142; 143]. These extremely diminish the electrical and thermal properties making it unsuitable for power-electronics die-attach.

Lateral flow approach: As a second approach in 'HotPowCon' project, the lateral flow approach was demonstrated as in Figure 19.e. Here the copper and solder are also applied separately in form of pastes. The copper paste is initially printed on the substrate followed by component placement, the solder is then made to flow laterally between the chip and substrate [141]. In this case, it was found that gaseous activation of the copper deposits was inevitable. Upon activation with liquid flux inside the copper deposits locally large amounts of gas, which require a rearrangement of the Cu particles and thus cause pores in the compound. In addition, there is a risk that activation is not fully successful and non-wettable areas remain in the form of pores in the copper deposit. For a particularly low void content, the application of a pressure variation during soldering is recommended [144]. The cross-section images of the followed approaches are given in Figure 20.

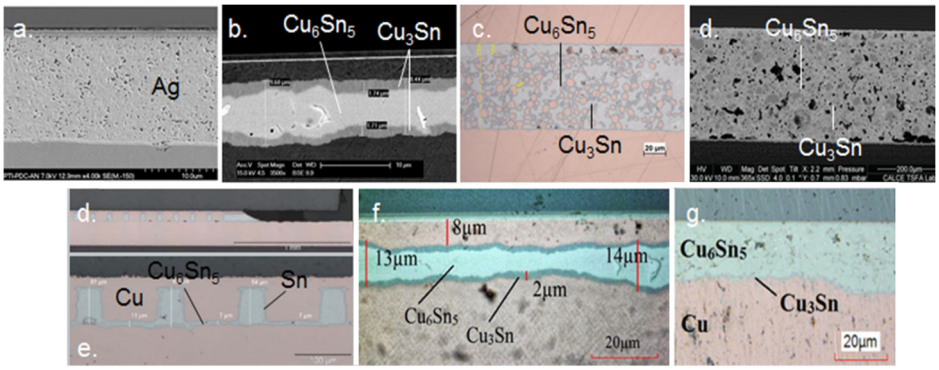


Figure 20: Overview of the high-temperature die-attach techniques presently followed a. Ag-sintering with low porosity; b. TLPB [17]; c,d. Composite solder [132; 139; 145]; d.e. Topology approach [134]; f.g. Thin-solder layer FAPS approach [131].

3.2.2 Investigated Approaches for Paste-based and Preform-based TLPS

As part of this thesis work, five different approaches were investigated to understand the TLPS mechanism, process complexity, material and process influences for the applicability in power electronics production. Three approaches are paste-based (A1a, A1b, A2) and two approaches are preform-based (B1, B2) for varying interlayer heights as shown in Figure 21. Table 7

gives an overview of the strategy followed in the production of TLPS interconnects for the Cu-Sn bimetallic system as interconnect material. The approaches A1a and A1b are investigated as part of project 'ProPower'. The related publications on the approaches are found for approaches A1a, A1b [131; 146; 147; 148; 149], A2 [150], B1, B2 [151].

Table 7: Overview of the procedure and the strategy followed in this thesis

Approach	Procedure	Interlayer thickness (µm)	Expected bondline thickness (µm)	Strategy followed
A1a, A1b	Paste based TLPS	20 - 25	8 - 12	Stencil paste printing
A2	Plasmadust enhanced TLPS	50 - 70	30 - 40	Stencil paste printing + Cu-Plasmadust
B1	Preform based TLPS	20 - 25	8 - 12	Preform placement
B2	Preform based Thick-film TLPS	65 - 75	30 - 40	Preform placement

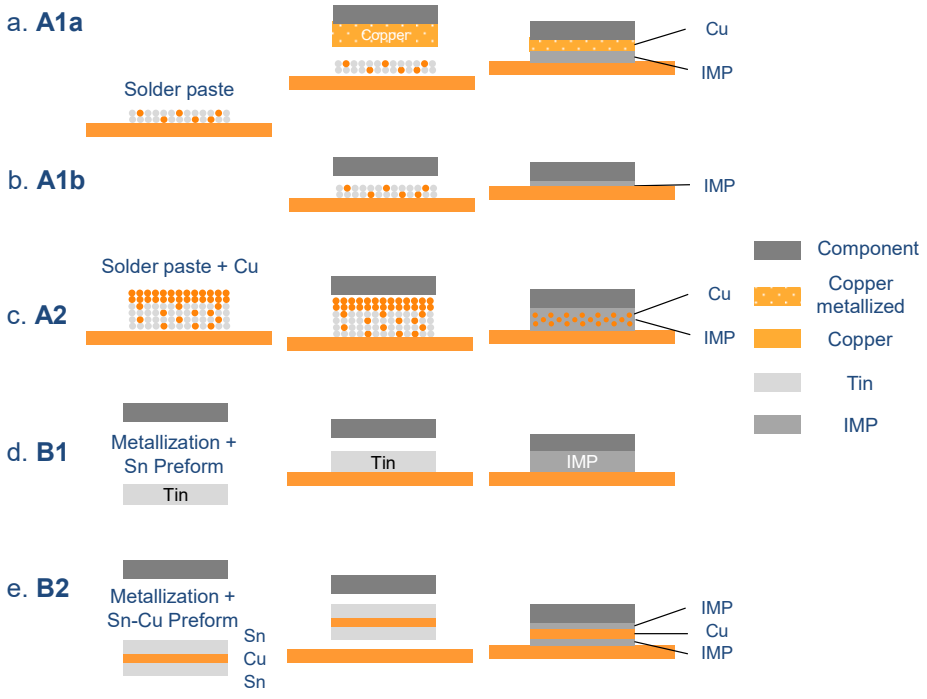


Figure 21: TLPS approaches followed as part of this work to automatize the production process through material modification and process optimization

The packaging concepts such as Ag-sintering or TLP Bonding (TLPB) are proven to be thermally stable and reliable in power cycling [73; 17; 16; 152; 133; 153], however require pressure-assisted bonding concepts and chip backside processing with suitable metallizations. With respect to the process chain optimization for mass production, these concepts require high investment costs and corresponding quality control. These demands for the optimization of the state-of-the-art power electronic process-chains for the economical production of high temperature interconnects.

Adaptability, requirements and complications

Another goal of the above explained composite approach was to convert the bondline into IMPs preferable Cu_6Sn_5 IMP. The required copper content w_{Cu} in Cu_6Sn_5 IMP is calculated by the equation 2 to 39.11%.

$$w_{Cu} = {6m_{ACu}}/{(6m_{ACu} + 5m_{ASn})} \quad (2)$$

Where m_{ACu} and m_{ASn} denote the atomic masses of copper and tin respectively. For full IMP transformation, a copper content of 39.11% is required. But the investigated solder paste $SnCu_{0.7}$ has only 0.41% of copper. The remaining 38.7% must be made available from secondary source. This corresponds to volume fraction of 22.1% In this thesis work, for the TLPS approaches A1 a/b and B1, the copper from the DCB and backside copper metallization is considered as secondary source. For the variants A2 and B2, the copper from the CAPM copper coating and cladded copper layer is considered as the source respectively.

The ProPower approaches A1a and A1b are the closest to conventional soldering. To ensure a full IMP transformation, a 20 µm thin layer of solder paste with fine filler particles is applied as interlayer. Since solder pastes are typically with 50% volume fraction of metal powder, the result is a roughly 10 µm thin solder gap [131]. This rough calculation is only valid for a specific stencil opening which corresponds to the bottom interconnect area of the chip. If the substrate is sufficiently smooth and a sufficiently low void content is reached, the entire solder gap can be converted into IMPs. The paste-based TLPS is still laborious and needs optimisation for mass production compared to standard soldering. These involve addressing of the solder paste printing defects, void formation and other production related costs. For the paste-based TLPS, a stable paste application process for printing thin layers of 20 µm is required and is not well established. For printing of pastes, the state-of-the-art paste application is limited down to 60 µm with stencil printing for solder materials and around 20 µm with screen printing in thin-film technologies [154; 155; 156]. The solder materials

however due to filler metals are not printable with screens for thin layers. This is due to the complexity of the designs to produce stable mesh systems capable of squeegee pressures during printing. In this work, the application of paste materials with metal fillers is investigated with stencils down to 20 µm thickness.

Preform-based solders however offer advantages with respect to process optimization, flexibility and cost reduction. For the preform-based TLPS, preforms of tin as LMM with thickness of less than 20 µm are required. However, the handling of such thin preforms is relatively difficult in production perspective. As part of the thesis, TLPS complaint preforms based on Cu and Sn are developed and used in the process development. A high quality of conventional solder connections can be obtained by the fluxless soldering of the assemblies where pore-free joints are achievable [157; 158].

Percolation theory for the copper content in the interlayer material

For the composite solder approach, the percolation theory was considered as the explanation for obtained high void content and unsuccessful IMP formation. This theory explains the formation of clusters or contiguous areas in randomly occupied structures before spreading of fluidic LMM through the HMM particle matrix. A solder paste deposit is a randomly arranged metal particle usually copper and tin in case of $SnCu_{0.7}$ with flux material in the cavities. According to this theory, the probability of a path formation of contagious copper spheres in the entire structure increases with a certain proportion of copper spheres. This fraction was called as percolation threshold. [159]

The copper particle weight content in the total quantity is denoted by 'p_c'. 'Φ_c' represents the volume fraction of the copper at the total volume from which percolation occurs. Both sizes are related to each other by the packing density 'f' of the composition as in equation 3:

$$\Phi_C = p_C \cdot f \tag{3}$$

During the thermal treatment, if the copper particles come into contact and form clusters with tin or IMPs, the component stays at same height as placed hindering the sinking of component and void-reduction. If this happen from substrate to component, a high void percentage is to be expected. Since packing of the random particles or spheres can have a packing density of at least 64% [160], it is impossible to achieve a void content of less than 36% in the volume of the solder joint with a copper content above the percolation threshold. The percolation threshold for packing of the random particles or spheres with a packing density of 59% was determined in

simulations with a volume fraction of 18.3% [161]. Though the exact packing density of solder paste deposits has not yet been determined, it is also assumed to be 59% as above. Consequently, a percolation threshold of 33.23% mass fraction of the copper (equivalent to a volume proportion of 18.3%) is obtained for solder paste deposits according to equation 2. This value applies to a cube-shaped total volume with an edge length which corresponds to ten times the ball diameter. In the experiments described above with composite solder approach, copper powder of grain size 3 i.e. type 3 with a mean ball diameter of 30 µm was used. The solder paste was printed with a 150 µm thick stencil. Thus, the height of the solder paste deposits is at most about five copper ball diameters.

The smaller the volume under consideration, the more frequently percolation occurs at lower levels [159]. As a result, it is advantageous for the composite soldering approach to use as fine copper powders as possible. This corresponds also to the fact that the experimentally determined limit of 20% mass fraction of the copper is lower than the value of 32.23% estimated from the literature values. Furthermore, in the present considerations, the movements of the solder paste deposit caused by the outgassing of flux components were not taken into account. These motions increase the likelihood of formation of individual clusters of contiguous copper particles.

As summarized from the 'HotPowCon' project, the composite solder approach thus makes two absolutely imperative demands:

- Before the melting of the solder, no percolation may occur, in order to allow a reduction of the component height by a maximum of 50%.
- After melting, percolation must occur in order to establish a sufficiently strong connection between intermetallic phases between substrate and component.

Both demands are indispensable and contradict each other. For this reason, no interconnection with low voids, which is composed completely of intermetallic phase, could be produced with the composite solders [130].

Addressing these complications, the approach A2 was investigated to check the IMP formation for higher copper content. However, the solder paste used was very fine (type 7) with additional copper supplied from the CAPM copper coating approach with copper particle sizes from 200 nm to a maximum of 5-10 µm.

3.3 Influential Factors

The process conditions in the diffusion soldering are dominant and influential in transforming the complete interconnect material into IMPs. The influential parameters in the diffusion soldering for a full IMP transformation are arranged into an Ishikawa diagram as in Figure 22. The time required for the IMP transformation is proportional to the interlayer thickness i.e. the diffusion distance. The diffusion based growth velocity '*d*' of the IMPs follow the following equation (4):

$$d = k \cdot \sqrt{t_{peak}} \tag{4}$$

The diffusion parameter k is a material-specific parameter (e.g. diffusivity) whose temperature dependence can be expressed through the following Arrhenius equation (5) [7]:

$$k(T) = k_0 exp\left(-\frac{Q}{RT}\right) \tag{5}$$

Where k_o is a pre-exponential constant, Q is the activation energy for diffusion, R is gas constant and T is absolute temperature. From the above equation it can be inferred that large activation energy means relatively small diffusion coefficient. It can also be observed that there exists a linear proportional relation between (ln k) and (1/T). Thus by plotting and considering the intercepts, values of Q and Do can be found experimentally.

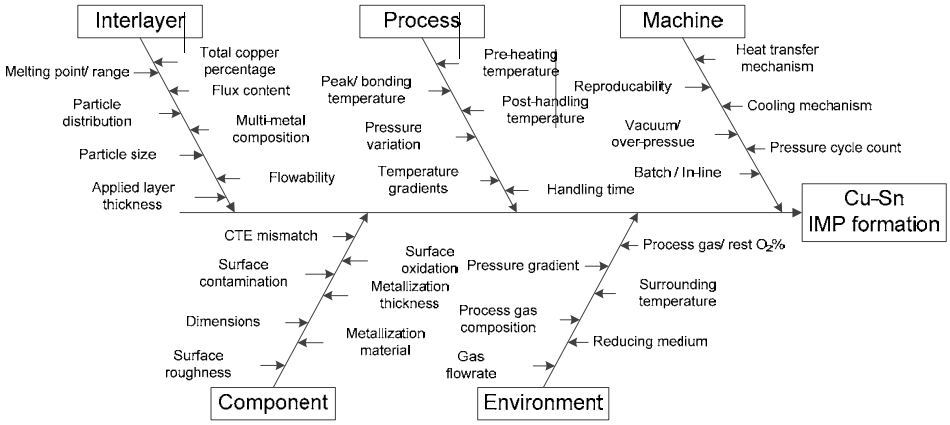


Figure 22: Ishikawa diagram showing the influential factors in the Cu-Sn IMP formation in production perspective.

Critical interlayer thickness

According to the above equations, the diffusion distance to be overcome is the interlayer gap between the parent materials i.e. substrate and component. For example, in case of chips with copper metallization, the diffusion distances drop to half, as the diffusion starts from both sides of the interlayer. Given the material parameters k_0 and Q, the theoretical process time can therefore be calculated as a function of interlayer height. In this work, the variants without pressure were mainly investigated with the aim of implementing this technique into production through conventional manufacturing equipment. The optimization of the thermal treatment and modification of the material composition plays a major role. The selection of the interlayer thickness is also very critical to the diffusion process. The critical thickness of the interlayer required is determined by the biggest intermetallic grain possible. When using lower thicknesses, contact between the parent components in the pre-melting phase is possible due to the pre-melting solid-state IMP growth which is interdependent on the surface roughness. There could be deficit in interlayer material near to IMP grains for the diffusion process when further substrate material i.e. Cu starts reacting. This can be due to the existing stiff grains from the heating period leading to void formation in the bondline. Literature suggests an interlayer thickness slightly above the critical thickness to secure the reliability but also keep the processing time small. Studies also suggest that an increase in heating temperature allows to increase the interlayer thickness as well as reducing the bonding time [46; 15].

During the initial phase of heating, the interlayer material starts diffusing into the parent metal. The magnitude of the diffusion depends upon the specific material combination. As all solid-state diffusion rates increase upon heating, consequently, the heating rate and interlayer thickness can significantly decrease the interlayer width. This is observed in fine-pitch application, where limited interlayer material is available. In some rare cases with less interlayer material, the complete material can be dissolved before the melting temperature of the interlayer is achieved. The critical interlayer thickness also depends on other variables such as bonding pressure, solid/liquid surface tension, surface roughness of the parent metal and intermetallic formation [72; 96; 152]. The bonding temperature is completely limited by the microstructural stability of the parent metal [124; 162]. The literature describes the bonding temperatures vary from the optimal bonding temperature to just above the melting points [163] or the bonding temperatures as high as allowed by the parent metal [164; 165]. The

intermetallic regions in a phase diagram, which tend to slow down the diffusion rate, can be avoided by raising the temperature [166].

The main idea was to produce a solder connection with complete intermetallic phases at chip-substrate interface. In a series of experiments, parameters were modified for realizing a thin-film TLPS joint <20 µm. The TLPS processes have been introduced through several works, but the information on void formation during the process was not investigated or demonstrated. For the implementation of TLPS interconnections, the technology or the method of production must also be portable for short time to market. In this work, the realization of TLPS joints with convectional reflow mechanisms used in electronic production processes is discussed and demonstrated. The optimization of temperature and pressure profiles for void reduction and intermetallic phase formation are briefly explained.

4 Machines and Materials

For the experiments conducted in this research work, the production equipment at Institute FAPS in electronics production laboratory in Nuremberg is used. The solder pastes and solder preforms were supplied by the material suppliers Heraeus Deutschland GmbH at Hanau, Germany and Pfarr Stanztechnik GmbH at Buttlar, Germany respectively. The case study analysis was conducted with the production equipment of Institute FAPS and at the R&D facilities of a power electronic module supplier in European and Asian regions namely Powersem GmbH, Schwabach, Germany. The detailed information on the materials, machines and the process parameters is given in the following sub-chapters.

4.1 Printing and Evaluation of the Interlayer Materials

The main goal of the work was to check the feasibility of the production of TLPS interconnections with varying bondline thickness and implementation with conventional (power) electronics production equipment. For this, the stencil printers, 3D-solder paste inspection, component placement machines and various soldering machines were used.

Generally with screen printing, very thin layers can be printed, however the printability is limited to viscous pastes like adhesives or sintering pastes. For printing of solder pastes, screen printing is not appropriate due to the clogging of the mesh with solder particles and required corresponding post-cleaning. In this work, for the printing of very thin layers of solder layers, stencil printing was selected. The deposition of solder pastes was performed by the DEK 'Horizon 265' stencil printer as shown in Figure 23.

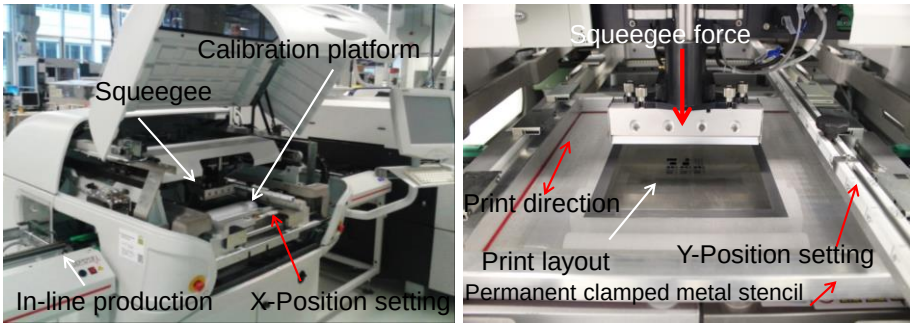


Figure 23: Solder paste printing equipment DEK Horizon 265 at Institute FAPS with 20 µm permanent clamped metal stencil.

The process windows for printing of very thin solder layers of 20 µm, 60 µm and 110 µm are explained in detailed in the next chapter. The stencil printing was done with aluminum blade squeegee with 45° angle. A reliable paste printing process was necessary for printing of solder pastes with very fine particles of Type 6, 7 and 8 with thin stencils from pad sizes ranging from 5 to 140 mm².

Cold-Active Plasma Metallization (CAPM) technology

The CAPM technology or also called Plasmadust technology is based on cold active atmospheric plasma beam in combination with a nano-scaled metal powder. In the plasma nozzle a carrier gas, e. g. nitrogen, is pushed to plasma by an electric arc. Additionally the copper powder is carried by a nitrogen gas flow into the plasma beam and is sprayed out of the nozzle. The powder melts due to the high energy of the plasma and the combination of plasma gas and melted powder coats the substrate surface [167; 168; 169]. The main objective in the TLPS A2 approach was to coat copper powder on the solder deposits by means of CAPM technology [150]. The additional introduction of copper particles in the printed solder deposit is intended to accelerate the formation of IMPs during the soldering process. This methodology promises controlled and uniform thickness of copper particles onto the solder deposits. Thus, it is expected that the diffusion processes are homogeneously distributed in the liquid solder melt significantly. The procedure, process development and results are discussed in the further chapters in material development. The used equipment of CAPM is shown in Figure 24.

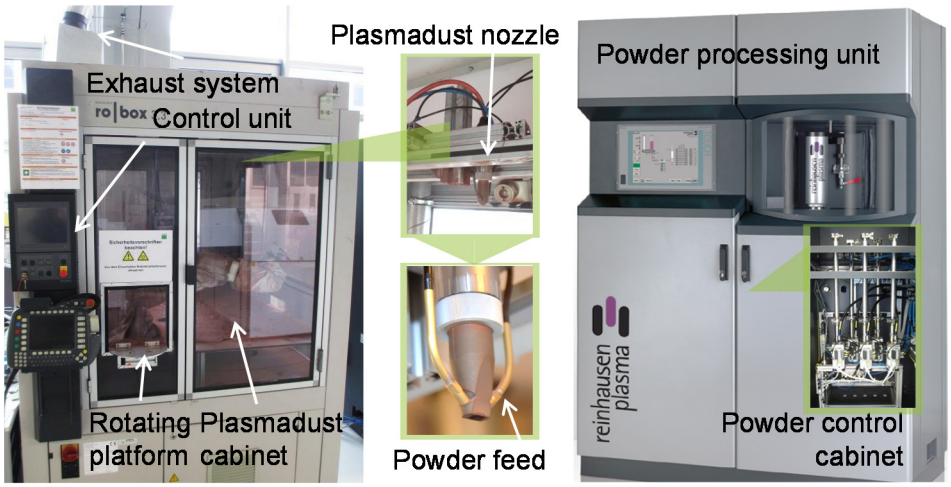


Figure 24: Components of CAPM/ Plasmadust® equipment at Institute FAPS used for the copper powder treatment of printed solder paste.

Kohyoung 3D-solder paste inspection systems

For monitoring and evaluation of the solder paste printing, the 3D-solder paste inspection (3D-SPI) systems from Koh Young Technology Inc. namely KY-3020T and KY-3030VA were used. The KY-3020T is an offline tabletop system and the KY-3030VA is an in-line serial system. Both the systems used in this work are shown in Figure 25.

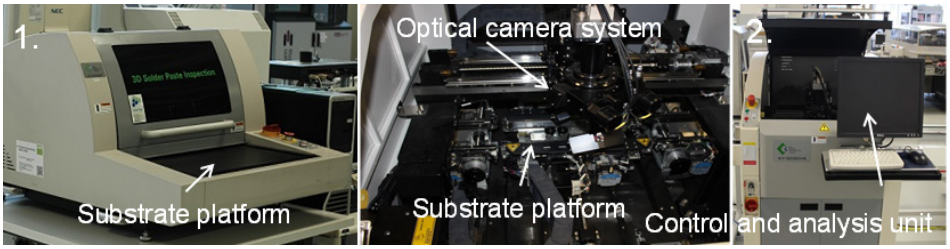


Figure 25: Components of the used 3D-SPI Systems (1) KY-3020T and (2) KY-3030VA for analysis of printed solder paste.

In the present study, the devices are mainly used to evaluate the quality of the printed paste deposits and also for the coating quality of the CAPM method. The surface topography, the absolute height and paste volume of the solder deposits, the homogeneity of the printing and coating process were evaluated. Both systems have a z-resolution capability of 0.37 µm and under operational conditions deliver a height resolution of 2 µm for KY-3020T and 1 µm for KY-3030VA respectively.

4.2 Soldering Techniques and Quality Analysis

Based on the heat transfer or functional principle, three different variants i.e. vacuum vapor phase soldering, overpressure convection soldering and heat conduction soldering were tested to understand the voiding characteristics and IMP formation. Here each of the techniques was selectively optimized initially for void-free soldering and followed by void-free TLP soldering. Based on void reduction mechanisms as shown in the Figure 26, the techniques followed are with pressure difference above or below atmospheric pressure.

Vacuum vapor-phase reflow soldering (VVP):

As the first variant, the condensation-based batch soldering machine 'IBL VAC645' as shown in Figure 27 was considered. It is constructed as a two-chamber system for IR-preheating and de-condensation/ cooling in the first chamber and for pre-heating and peak temperature in the second chamber under an inert atmosphere. The temperature and time control of

the soldering profile including pre-heating is performed by division the second chamber into 10 vapor levels and 20 program steps in addition to the main soldering step under vacuum. The chosen combination of holding time in one step and the corresponding height position of the workpiece carrier is set according to the heating or cooling gradients and holding temperatures. The second chamber is included with rapid-cooling system (RCS).

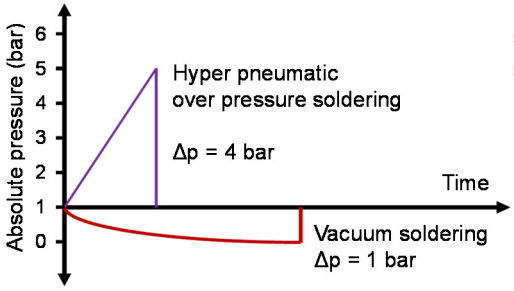


Figure 26: Void reduction mechanisms showing the traditional vacuum technique and the new variant of hyper-pneumatic pressure variation. [170]

A typical vapor-phase solder profile is shown in Figure 28. The vacuum is activated at the end of the peak zone to reduce the voids in the solder joint. The vacuum can be controlled in various levels down to 15 mbar (Step 2). It is however very important to release vacuum after the solder is cooled below the liquidus point. The control of the solder profile is relatively complex compared to any convection based oven. But once the profiling has been done for a particular temperature or product, the technology offers an energy-efficient soldering technique with reproducible solder profiles and results.

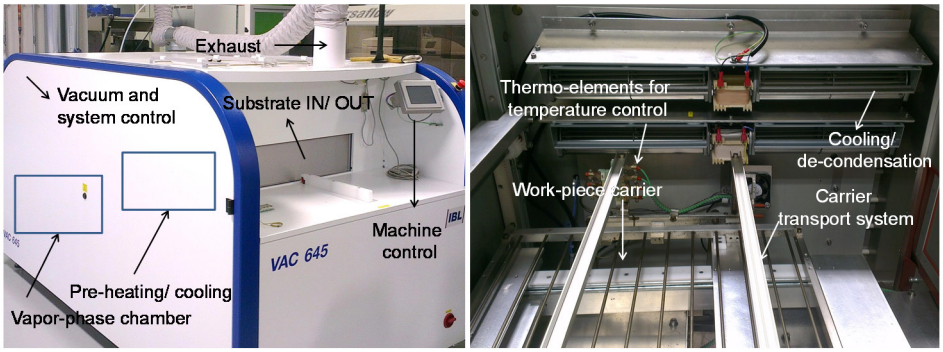


Figure 27: Components of vacuum vapor-phase soldering oven IBL VAC645 showing the work-piece carrier on the right.

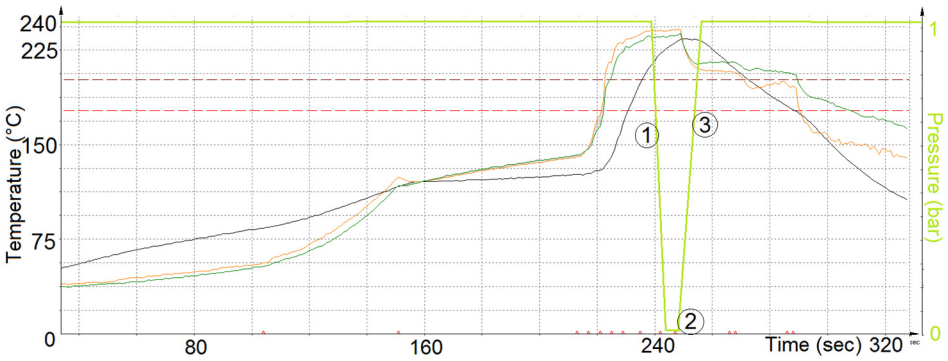


Figure 28: Typical vapor-phase solder profile showing the pressure change down to 15 mbar at peak-time.

Generally in conventional vapor-phase soldering, galden medium of 240 °C is used. But in this work, the above machine was first commissioned for usage in soldering of power-electronic assemblies and as heat transfer medium, the new galden material with a boiling point 260 °C was used. After the profiling for void-free solder connections, the profiles have been modified for TLPS.

Over pressure convection soldering machine (OPC):

As the second variant for the investigations towards over-pressure TLP soldering, the convection-based in-line reflow soldering machine SEHO MaxiReflow 3.0 HP was used. In this machine, during the temperature profile mainly during molten phase of the solder at the peak temperatures, over-pressure of maximum relative pressure of 4.2 bar can be generated through a hyper-pneumatic chamber. The concept of building up multiple pressure cycles is termed as Squeeze-Release-Squeeze-Freeze (SRSF) cycle. This chamber has a capacity of 240 liters and a pressure difference between the void and the surrounding can be generated up to four times. A picture of the machine and the over-pressure chamber is shown in Figure 29. It has 6 pre-heating zones, 2 peak zones, and 2 cooling zones operatable with air or nitrogen. The two peak zones i.e. chamber positions are named as cp1 and cp2. In addition to the hot-air blowers, quartz-based heating elements are built in the pneumatic chamber to stabilize the temperature variations due to the pumped air during pressure build-up.

The temperature profile in the machine is so installed, that the solder will be in molten state before entering the pneumatic chamber. The components stay primarily for few seconds at normal pressure to ensure complete natural outgassing of the gasses formed. Then at chamber position 'cp2',

these are subjected to over-pressure up to 4.2 bar relative pressure decelerating the new gas formations in the solder (Squeeze: S). The existing pores or the trapped gases are exhausted out of the solder joint during the pressure release leading to reduced voids (Release: R). This pressure cycle can be repeated for up to 2 times to ensure complete gas exhaust (multiple SR). Finally the final pressure is built-up (Squeeze: S) and moved into the chamber position 'cp2' for solidification (Freeze: F). An important step here is that the before releasing the pressure, the components are to be moved into the position cp2 to ensure a void-free solder connection. A typical temperature profile with over-pressure for a lead-free solder material is shown in Figure 30.

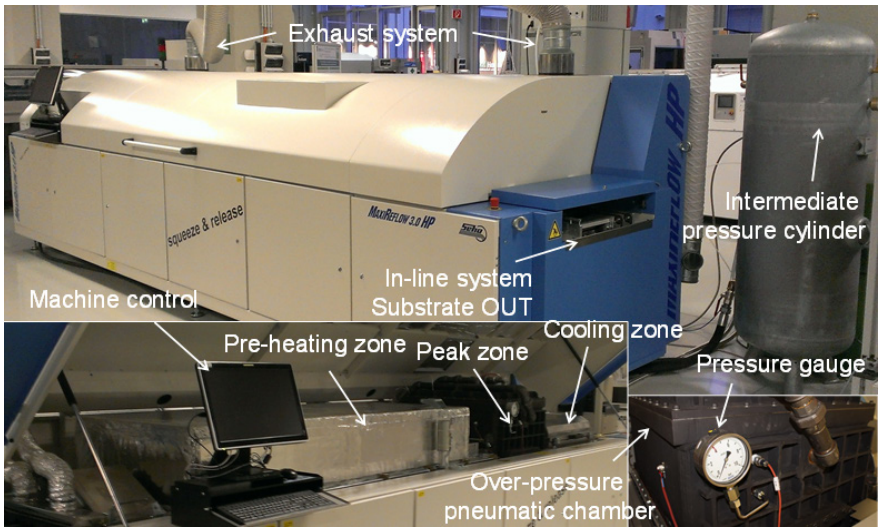


Figure 29: Components of the SEHO Maxi Reflow 3.0 HP showing the pneumatic chamber and the temperature zones.

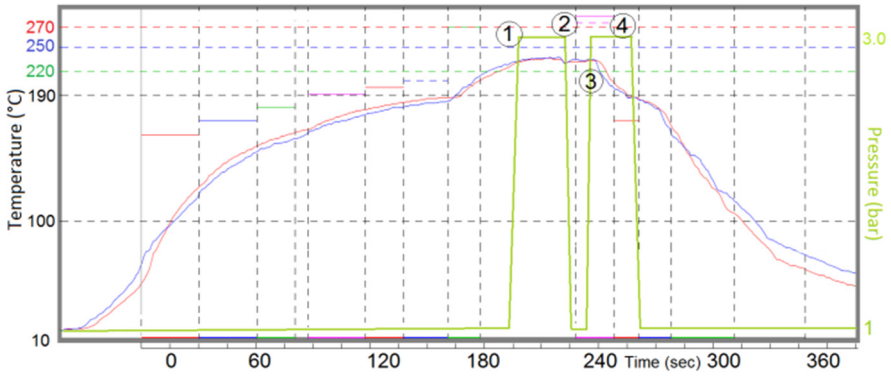


Figure 30: Temperature profile of over-pressure soldering oven measured at component and substrate showing the pressure change up to 4 bar at peak time.

The machine concept is relatively new compared to the vacuum-based convection reflow soldering systems. The outcomes of the influence on the over-pressure are not yet completely explored. In this thesis, the influence of the variation in the relative pressure is investigated not just for the void-reduction, but also for the IMP development. The above explained two machines were newly commissioned at Institute FAPS as part of this research work in power electronics production and diffusion soldering.

Conduction based flux-less soldering (CFL):

As the third variant, the conduction-based inline soldering machine from PINK GmbH Thermosysteme namely 'VADU 300XL' had been used at the facilities of Powersem GmbH, Schwabach. The system is divided into three sections mainly pre-heating, main heating and cooling zones. The process gases here are mainly formic acid and forming gas for fluxless soldering. The machine has a capability to generate vacuum less than 2 mbar and over-pressure slightly over 1.3 bar. For the soldering of the assemblies, available mechanical jigs were used for uniform heat transfer and alignment of the components. The modification of the mechanical jigs and optimized profiles for the developed preforms for TLPS technology are explained in the next chapters. An overview of the used soldering systems is given in Table 8 and the process-related influences are explained in sub-chapter 7.1.

Table 8: Overview of the used soldering systems

Soldering technology	Machine used	Void-reduction technique	Pressure settings
Condensation	IBL VAC 645	Vacuum	15 mbar
Convection	Seho MaxiReflow 3.0 HP	Over-pressure	4 bar
Conduction	VADU 300 XL	Vacuum / Over-pressure	2mbar / ~1.3 bar

4.2.1 Non-destructive Optical and Destructive Analysis

In-situ X-ray analysis: For the analysis of the pores, the in-situ X-ray analysis system developed at the IAVT, TU-Dresden was used in the experiments as part of the ProPower Project [171; 172]. This allowed a deeper understanding of dynamic behavior of the solder material during the solder process. Parallelly, the effects of the pressure changes are also visible for interpretations for profile optimization.

The test setup was successfully developed by Mr. Klemm [173], which has the capability to record the solder process at frame rate of 30 Frames/sec for the analysis of the voiding with change in flux materials and solder height with respect to pressure changes. The overview of the test set-up and the internal construction are shown in Figure 31. The chamber had an indentation for better absorption on top of measurement area. The test sample substrate with printed solder paste and component is placed within the aluminum chamber, where the temperature and pressure input is monitored and controlled through the input program to the control electronics of the chamber. The heating element under the test sample provided the heat through conduction and the PT-1000 sensor supported in the monitoring of the temperature on the substrate near to the test area. In this work, the same test set-up was used for the preliminary voiding analysis mainly standard profiles and peak extended profiles with pressure changes for thin paste heights. Further the interpretations for diffusion soldering were also performed for further optimization. The size of the setup had to be small for an efficient and flexible sample change so a passive cooling of the heating plate for a simple construction was used. Figure 32 shows a series of in-situ x-ray pictures for a semiconductor chip of size 10 mm x 10 mm [172; 174]. The in-situ measurement setup was placed inside the X-ray machine with following requirements:

- low and homogeneous absorption of X-ray radiation in the beam path perpendicular to the measured area
- low height as possible above the sample for a high magnification
- pressure resistant from -100 kPa to +300 kPa (relative to ambient pressure)
- feasible for practical soldering profile testing with a heating rate of 2 K/s and a maximum temperature of 250 °C.

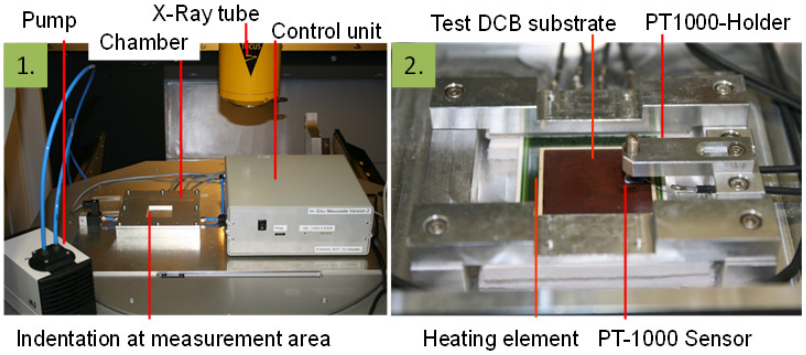


Figure 31: In-situ test setup developed by Klemm (1); Internal construction of the set-up for the control of the temperature and pressure profile (2)

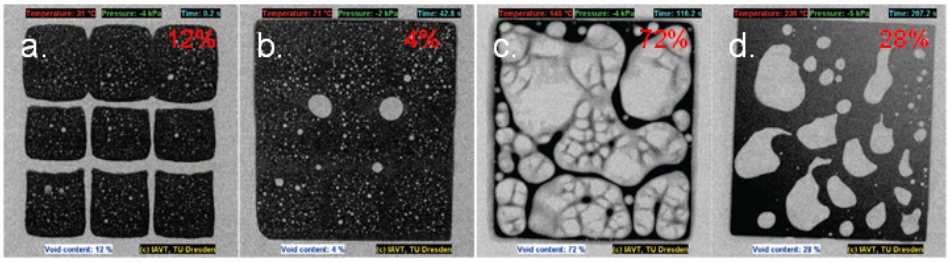


Figure 32: In-situ X-ray recording a. after the component placement; b. start of solving agent evaporation; c. vaporization of solving agent; d. gas production after melting of solder [172].

Optical inspection: For the X-ray analysis, the machine from company Nordson Dage namely XD7600NT with X-plane inspection as shown in Figure 33 was used. Here the X-ray images were measured for the void percentages for all the produced solder joints. For the microscopic analysis, the 3D-laserscan microscope from company Keyence namely VK-9710 as shown in Figure 33 was used.

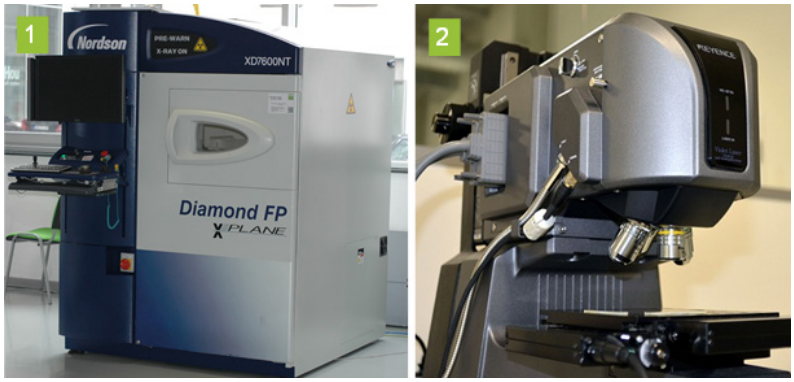


Figure 33: X-ray machine and Keyence laser-scan optical microscope at Institute FAPS used for optical analysis.

For evaluation of the cross-sections, the produced test samples were prepared for metallographical analysis. The scanning electron microscope (SEM) with electron dispersive analysis (EDX) and focused ion beam (FIB) analysis was performed together with the partner universities and institutes.

Shear testers: To study the mechanical strength of the TLPS joints produced, room temperature and high temperature shear tests of the components were performed with shear testers from XYZTEK Condor 150-3 and Nordson DAGE namely 4000 Plus with heating module up to 450 °C respectively. The pictures of the machines used are shown in Figure 34. The shear

parameters used here are maintained constant for all the samples. The parameters used were shear velocity of 250 µm/s and shear height of 50 µm for component height of 250 µm and bondline thickness of 25 µm (i.e.10% of component height + bondline thickness). The shear doses of 400 N and 2000 N are used for shearing components of various sizes and heights. The tests were however limited to maximum surface area of 25 mm².

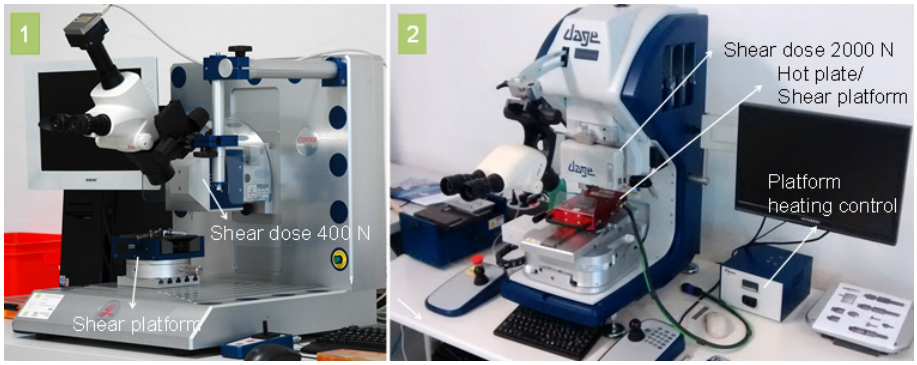


Figure 34: Shear testers XYZTEK Condor and Nordson Dage 4000 with hot plate for destructive tests used in this work.

4.3 Materials for the Production and Analysis of TLPS Process

Various silicon components were used in the analysis of voids and IMP development. A few components with varying chip thickness and dimensions have also been tested for the warpage during the soldering process. The components used had either AlSiCu or Cu frontside metallization and as backside metallization either NiAg or Cu as shown in Table 9. The components had a passivation of photoimide on the frontside. For the tests and evaluation with void analysis and shear tests, dummy components with bronze basis were used. The components were with Cu and Ni-Ag metallizations specially prepared for the test purposes as shown in Table 10. The components with copper metallization were also used in the IMP analysis to check the influence of the heating profile with component height and interlayer thickness.

Table 9: Semiconductor components used with varying size, thickness and backside metallization.

	Component type: Silicon	Component size (LxBxH) [mm x mm x µm]	Avg. thickness (µm)	
			Frontside Al-SiCu variant	*Frontside Cu variant*
Front AlSiCu / Cu and Backside NiAg metallization	Resistor	2.30 x 2.30 x 500		-
	MOSFET	7.20 x 4.20 x 200	5	49 ± 1
	Diode 600V	9.20 x 5.44 x 70	3.2	80 ±1.2
	IGBT 600V	9.73 x 10.23 x 70	3.2	57 ± 1.2
	Diode 1200V	8.15 x 9.00 x 120	3.2	7 ± 0.4
	IGBT 1200V	7.48 x 14.61 x 140	3.2	14 ± 2.8
			Frontside Cu	*Backside Cu*
2 x Cu metallization	Diode 600V	9.20 x 5.44 x 70	62 ± 4	9 ± 0.6
	IGBT 600V	9.73 x 10.23 x 70	82 ± 2	11 ± 1

Table 10: Dummy components used with varying size and backside metallization

Component name	Component size (L x B x 250) [mm x mm x µm]	Backside metallization + Plating	Metallization thickness
DC1, DC2, DC3	2.5 x 2.5; 5 x 5; 10 x 10	Cu	15 µm
DN1, DN2, DN3	2.5 x 2.5; 5 x 5; 10 x 10	Ni + Ag	3 - 4 µm + >200 nm

Power-electronic substrates: The substrates used for the experiments are DCBs with 0.3 mm Oxygen-free copper (OFCu) conductor on both sides of the 0.65 mm ceramic alumina (Al_2O_3) base. The standard copper (SC) substrates had a surface roughness $R_z \leq 16$ µm and the Standard Ni-plated copper (SNC) and paula processed Cu-substrates (SPC) had a surface roughness $R_z \leq 5$ µm as shown in Figure 35. The properties and the measure roughness are given in Table 11.

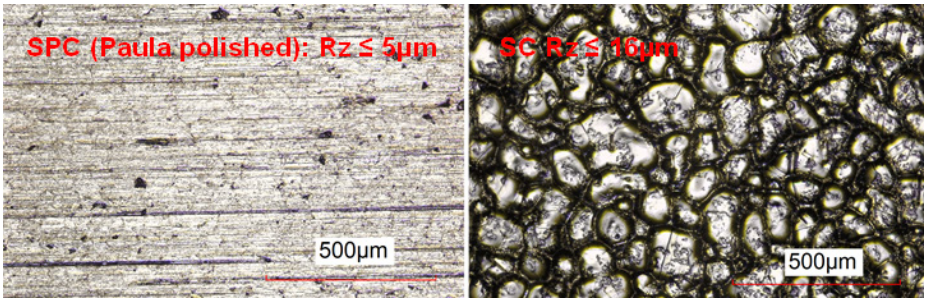


Figure 35: Microscopic images of the used power electronic substrates SPC and SC with corresponding roughness.

Table 111: Specifications of the power electronic DCB substrates used in this work.

Substrate type	**Name**	**Plating**	**Thickness (µm)**	**Roughness (R_a; R_z) [µm]**
Standard	SC	No plating: rough	-	≤ 0.48; ≤ 16
Paula[8]	SPC	No plating: polished	-	≤ 0.02; ≤ 6
Plated	SNC	Nickel	4 - 7	≤ 0.02; ≤ 6

Softwares:

COMSOL Multiphysics was used for the concentration gradient 2D-simulation of the Cu-Sn IMP formation. The used version was COMSOL Multiphysics (Class-kit License), Version 5.2. It is a universal software platform that enables the modeling and simulation of coupled or multi-physical phenomena using advanced numerical methods by means of differential equations. The module 'Transport of Diluted Species' was used to compute the concentration field in this work. The used methodology and modules are further explained in the sub-chapter 6.1.

MATLAB Software (Version R2013b) was also used along with COMSOL to evaluate the obtained results. The temperature profiles over time were generated as well as the obtained result of IMP formation in Cu-Sn was visualized.

[8] Paula processed DCB substrates are specially polished DCBs from Curamik electronics GmbH/ Rogers Corporation for lower roughness and uniformity of copper conductor.

4.4 Experimental Plan and Investigated Factors

As part of the research work, various experimental tests were performed to understand the material- and process-related influences in order to optimize the thermal treatment for the TLPS interconnections with goal of low-voids and full IMP transformation in the bondline. A timeline overview of the conducted experiments followed over four years is given in Table 12 Here the solder paste materials of $Sn_{99.3}Cu_{0.7}$ with flux type F645 were used with particles sizes of Type 6, 7, 8 on surface variants SC and SPC. The preform materials based on Cu-Sn and Cu-Sn-Ni were used on the substrate variants of SC and SNC. Depending on the objective of individual combination, the soldering techniques vacuum vapor phase (VVP), overpressure convection (OPC) and conductive flux-less (CFL) soldering techniques are used.

The investigations in the preparation of the assemblies for high-quality, reproducible results for various influences was relatively complex, as each and every part of the process step immensely influences the final void percentages and IMP formation. A high priority was given to the preparation of the samples and progressive work strategy in the statistical evaluation of the results. The multi-level planning concept was used to evaluate the influential parameters in individual test series. It allowed the iterative adaptation of the experimental parameters between the individual test series on the basis of existing experience values. Due to interaction of multiple process steps in production of TLPS interconnections, a rigid statistical experimental plan was relatively complex due to numerous individual factors in each process step as the thin-layer paste printing, component placement and thermal treatment. The followed approach allowed the selection of the individual components displaying the best results and combining with next factors of influence arriving to a reproducible conclusion of relevant parameters. An example is the preliminary selection of solder paste of $Sn_{99.3}Cu_{0.7}$ from the solder variants of Sn-Ag-Cu and Sn-Cu for the further experimentation. The selected solder paste composition from trail 1 is further analyzed with VVP soldering to understand the initial IMP formations with and without mechanical influence for thin bondlines in trail 2. After estimating the IMP thicknesses, the soldering techniques were investigated for void-reduction for Type 6 solder paste in trails 3 and 4. The influences of the metallization, chip warpage and void characterization for prolonged peak time were combined with further thermal and pressure profiling in trails upto 9 with combination of solder paste types and surface roughness. In trails 10 and 11, the material influences were tested for IMP formation

followed by CAPM process in trail 12. The temperature profiles were parallelly optimized with help of in-situ investigations for substrate roughness. Finally the temperatures profiles for the types of combination of preforms with CFL soldering were finalized. The product and technology case-studies were performed with the selected profiles according to the material combinations in final trails.

Table 12: Overview of the conducted experiments as part of the thesis work.

Trail Nr.	**Approach**	**Soldering technique**	**Used materials (interlayer, profile)**	**Accounted influence and goals**
1	A1	VVP	Type 6 SnAgCu	Silver in interlayer, defect analysis
2		VVP	Type 6 SnAgCu	Heat transfer direction and weight
3		VVP	Type 6 SnCu	Void reduction, multi pressure cycle, component size and metallization, interlayer thickness, chip warpage
4		OPC	Type 6 SnCu	
5		VVP	Type 6 SnCu	Prolonged peak time, component metallization, chip warpage
6		VVP	Type 6,7,8 SnCu, $R_z \leq 5$ µm/ 16 µm	Prolonged peak and post-handling, reduced post-handling temp.
7		OPC		
8		OPC		Reduced post-handling temp, solder process defects
9		VVP		
10		VVP	Type 6 SnCu, $R_z \leq 5$ µm	Influence of nickel, substrate metallization
11		VVP/ OPC	Type 7 SnCu, $R_z \leq 16$ µm	Chip warpage, metallization component size

12	A2	VVP	Type 7 SnCu	CAPM, influence of copper
13	A1/B1	In-situ	Type 6 SnCu, $R_z \leq 5$ µm/16 µm	Surface roughness, peak and post-handling time,
14	B1/B2	CFL	Preform SnCu, $R_z \leq 5$ µm	Preform thickness, wetting characteristics, Ni additive
15	B1/B2	CFL	Preform SnCu, $R_z \leq 5$ µm	Cladded preforms, IMP formation, wetting characteristics
16	all	VVP/ CFL	$R_z \leq 5$ µm	Product and technology studies

5 Development and Processing of the Interconnect Materials

In power electronics, generally solder pastes dominate as interconnect materials. Presently SnAgCu and Innolot solder pastes are used as die-attach interconnect material for the production of power modules. The fluxless soldering is usually presently used in the power electronic assemblies where very high quality is required. In case of diffusion soldering, the thermal treatment for the interlayers varies from conventional soldering. The energy transferred should be abundant for full IMP transformation. The approaches considered as shown in Figure 21 for the Cu-Sn bimetallic TLPS technique investigated in this work are mainly to check the feasibility for serial or mass production. Also the influences in the various process generated defects as summarized in sub-chapter 3.3 are parallelly taken into consideration. For this, the variations with respect to the materials were mainly in the procured interlayer material form i.e. thickness of the used paste and preforms. For TLPS with thin bondlines, the solder material is printed using stencil printing with height of 20 µm (A1a, A1b) and custom designed fluxless preforms with thickness of 20 - 25 µm (B1) were used. For bondlines greater than 30 µm, paste height of 30 - 40 µm and additional 20 - 30 µm copper particles were deposited on the solder before component placement (A2) and custom designed cladded fluxless preforms (Sn-Cu-Sn) with total thickness of 75 µm (B2) were used.

5.1 Preparation and Printing of TLPS enhanced solder pastes

The formation of IMPs mainly begins at the solder-substrate interface as explained previously between LMM and HMM during the initial phases of the thermal treatment. For the preliminary investigations for printing and IMP formation, the solder pastes $Sn_{96.5}Ag_3Cu_{0.5}$ and $Sn_{99.3}Cu_{0.7}$ Type 6 were used to check the influence of the additives like Ag. This can be observed through scanning electron microscopy (SEM) images of joints produced with standard soldering profile in Figure 36. It can be observed that the surface roughness has also influence on the phase formation rate. On the rough parts of the copper surface, the IMP formation mimics the peaks. In Figure 36.a, the Sn-Cu paste shows good phases without any hindrance with very good scallopial structures. An inclined growth rate can be seen where

the roughness is higher. However in Figure 36.b, formation of Ag_3Sn intermetallic hinders the Cu_6Sn_5 formation. Though Ag intermetallics increase the Cu dissolution in Sn at initial phases, they gradually reduce the growth rates of Cu_6Sn_5 and Cu_3Sn [175; 176]. Though the solubility of Cu in Sn-Cu solder paste is lower compared to Sn-Ag-Cu, the high process temperatures of 260 °C compensate the diffusion rate. The IMP formation at the NiAg backside metallization of the chip is relatively slow due to deficit of copper atoms for diffusion. Small clusters of Cu_6Sn_5 can be found at the interface.

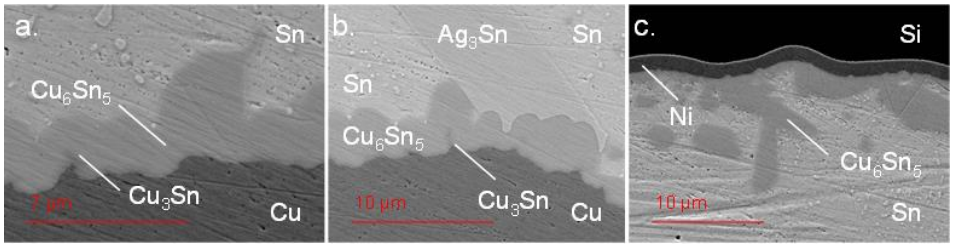


Figure 36: SEM+EDX images showing the influence of the silver and nickel in SnAgCu solder paste on the Cu-Sn IMP formation.

Figure 37 shows the cross-sections of a sample soldered with supporting pressure of 400 g on the chip and peak time of 5 min at 260 °C. It can be observed that apart from the crystal structures, Ag_3Sn islands hindering the Cu_6Sn_5 growth. Based on these results, for further investigations, the solder paste $Sn_{99.3}Cu_{0.7}$ was selected.

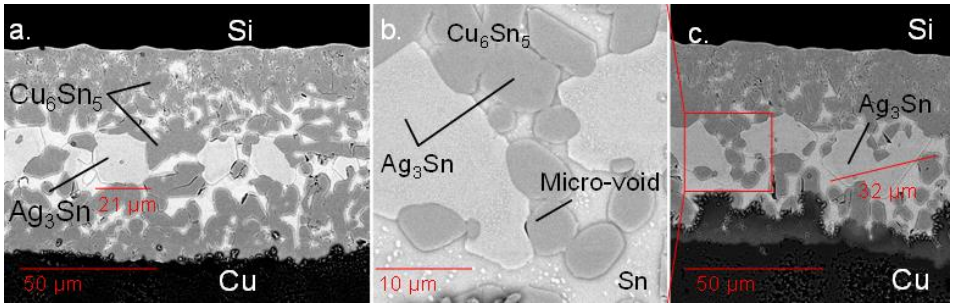


Figure 37: SEM+EDX images showing the influence of the Ag_3Sn crystal formation in SnAgCu solder paste on the Cu-Sn IMP formation.

In soldering technologies with solder pastes, various factors influence the final void content of the interconnection, as explained in the sub-section 3.3. For the approaches A1a, A1b and A2 i.e. paste-based TLPS, conventional solder materials of composition $Sn_{99.3}Cu_{0.7}$ of flux variant F645 and Types 6, 7, and 8 were used. The melting region for this composition was between 230 °C and 250 °C with solid content of 86 - 88%. Table 13 gives an overview

of the solder paste particles sizes for the used paste types. For the optimization of paste printing process for stencils of 20 µm thickness, particle sizes of < 20 µm were required. It must also be taken into consideration that the initial solid-solid interdiffusion is dependent on the metal grain size in contact with the substrate surface. It can be seen from the table above that the paste types above Type 6 are appropriate for the printing of the required thin layers.

Table 132: Overview of the metal particle sizes in the solder pastes

Type	Particle diameter ≤ (µm)	Greater than 1% (µm)	≥ 80% are between (µm)	≤ 10% are smaller than (µm)
1	160	150	100-75	20
2	80	75	75-45	20
3	50	45	45-25	20
4	40	38	38-20	20
5	30	25	≥ 90%: 25-10	10
6	20	15	≥ 90%: 15-5	5
7	15	11	≥ 90%: 11-2	≤ 1% < 2
8	11	10	8-2	---

For the tests, two stencil layouts were mainly selected, a 20 µm stencil layout with and without bridge structures and a second layout combining various apertures sizes corresponding to the used silicon and dummy components for 110 µm, 60 µm and 20 µm stencil thicknesses as shown in Figure 38. For the statistical evaluation of the printed pastes mainly the paste height and volume, the lower layout in Figure 38.a with apertures of increasing component pads was selected. In the evaluation using the 3D-SPI, the fiducials 1 and 2 were used as reference points. For the tests, it was required to find the optimal printing process parameters for the selected stencil thicknesses. For 110 µm stencil, the standard parameters as shown in Table 14 were used, however the optimization was required for the reliable paste printing process of 60 µm and 20 µm stencils. For the preparation of the assemblies with the paste printing, metal substrate carriers were built and used for all the stencil thicknesses as shown in the Figure 38.b.

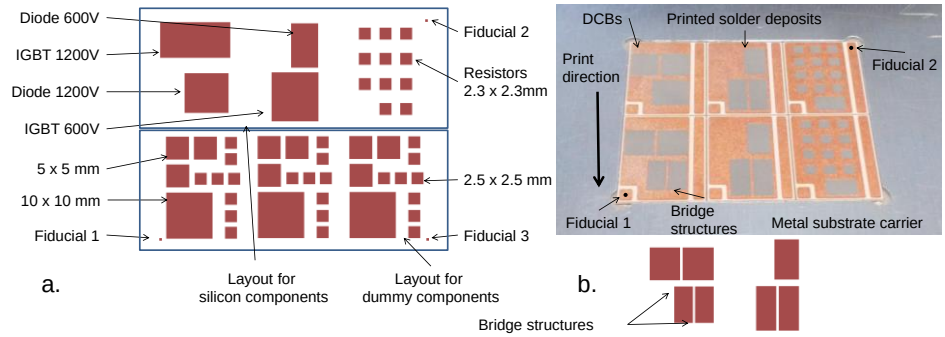


Figure 38: a. Stencil layout for silicon and dummy components for stencils of 20, 60 and 110 µm thicknesses; b. 20 µm printed DCBs with bridge structured layout.

The printed samples from the 110 µm and 60 µm stencils were used further in the copper particle treatment using CAPM process explained in sub-chapter 5.2 and preliminary IMP analysis as continued in sub-chapter 6.1 after 3D-paste inspection process. The KohYoung 3020 and 3010 systems at Institute FAPS were used for evaluating the paste height, volume and printing related defects. The main aim was not to optimize the printing parameters, but to investigate the interdependencies with the soldering process. So, the main focus was to achieve uniform and reproducible paste heights with the main influential process parameters [177].

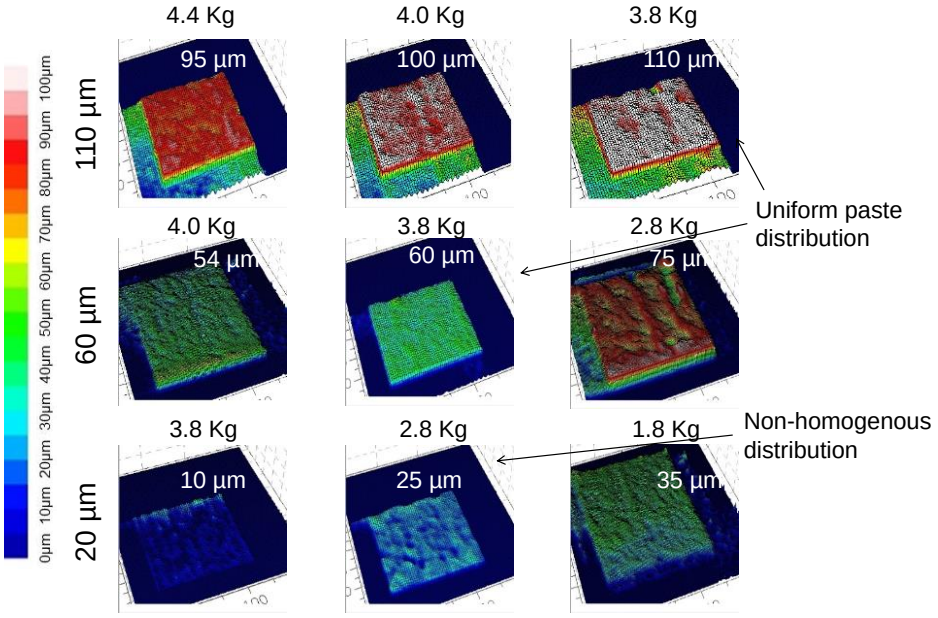


Figure 39: Paste heights of the printed solder pad size 2.5x2.5mm² with indicated stencils on SC substrates with $R_z \leq 16\mu m$.

Table 14: Tested paste printing parameters for varying stencil thicknesses.

Stencil thickness [µm]	Tested print force [kg]	Tested velocity [mm/s]	Selected parameters
110	4.0, 4.4	35, 40	4.0 kg, 35 mm/s
60	2.8, 3.0, 3.4, 3.8, 4.0	35, 40	3.8 kg, 35 mm/s
20	1.8, 2.0, 2.8, 3.0, 3.4, 3.8	30, 35, 40	2.8 kg, 35 mm/s

Here the printing squeegee force, printing velocity and the print count per substrate were mainly varied to obtain the required paste height and volume. Finally, the print force was selected keeping the print velocity constant at 35 mm/s. It can be observed from the Figure 39, that the paste height increases with decreasing squeegee force. The homogeneity of the paste was dependent on the substrate roughness. It can be seen that the paste application was uniform for 60 µm and 110 µm. An overview of the printing parameters for the stencil thicknesses 20 µm, 60 µm and 110 µm are given in Table 14.

For smaller pad sizes, the printing characteristics were excellent with paste volume between 95 to 110 %. However for large-area apertures, a secondary layout was also considered to see the influences of bridge design in the layout to optimize the printing process as shown in Figure 38.b. The bridge structures tested were designed considering mainly two aspects. On one hand, the bridge structures should be small in size and number, to obtain a homogenous paste application without significantly changing the total paste volume on the pad and the void content in the consecutive production process. On the other hand, the bridges must be placed precisely considering the total pad dimensions and the printing directions. The thin stencils are prone to more damage due to such designing errors. A bridge structure perpendicular to printing direction damages the stencil and the resultant printing process extremely. This could be due to the bending or flipping of the structures. For the layout shown in Figure 38, bridge structures were integrated for apertures sizes greater than 50 mm².

Figure 40 shows the images of the pads printed with 20 µm stencil with and without bridge structure with pad size of 100 mm². The used solder paste was Type 7 on substrate SPC of $R_z \leq 5$ µm. The image on the right shows that the printed paste thickness was homogenous at height of 22 µm. On the left without bridge, due to continuous squeegee force on the total aperture, the paste volume was significantly reduced from edges to center

with solder height difference of around 14 µm. It can be observed that the paste volume also increased along with the length of aperture in printing direction.

For the stencils 110 µm and 60 µm, one print per substrate was sufficient due to optimal parameter combination and printed paste volume irrespective of aperture sizes. But for the 20 µm stencil, for aperture sizes above 25 mm², a double print per substrate was required to homogenize the paste volume over the whole pad area. It should be noted that the paste type 6 and substrates SC and SPC were used for the stencil printing tests and parameter optimization. The 20 µm stainless steel stencil used for the printing tests and was very sensitive in terms of mechanical stability compared to 60 µm and 110 µm stencils. Even a misalignment or excessive pressure extremely damaged the stencil with scratches and defects. The roughness of the substrate also damaged the stencil when excessive squeegee force was used. So, a low squeegee force below 2.8 kg was selected based on the obtained paste volume and height.

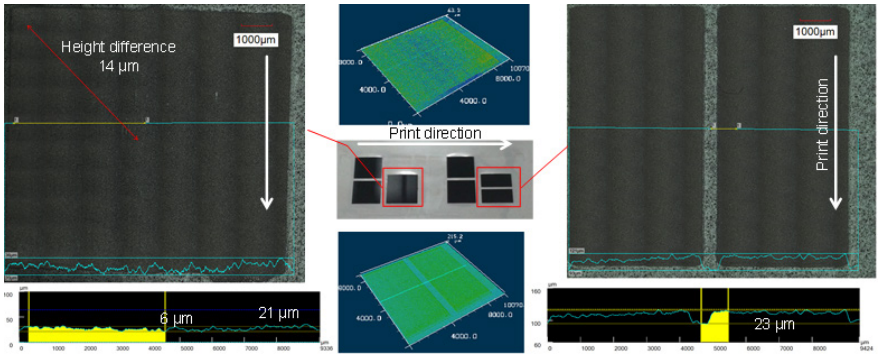


Figure 40: Comparison of printing characteristics without and with bridge of 10x10 mm pad with 20µm stencil.

Figure 41 shows the height distribution of 10x10 mm² pad with printing direction and count. As explained above, double print was considered for large area apertures, this stabilized the uniform application of pastes. In Figure 41.a,b, for one print direction, the paste height varied significantly with print force due to the scooping effect. Here the paste though rolls into the apertures, and is scooped away at the same time. As with increased squeegee force, the scooping effect significantly increased reducing the gap between the squeegee blade and substrate. For smoother surfaces, the solder particle size plays also huge role, where the gap must be at least 15 µm for Type 6 solder paste. The double print parameters of forward/backward squeegee pressures 3.0/2.8 Kg and 2.8/2.8 Kg were used as final parameters for substrates SC and SPC respectively.

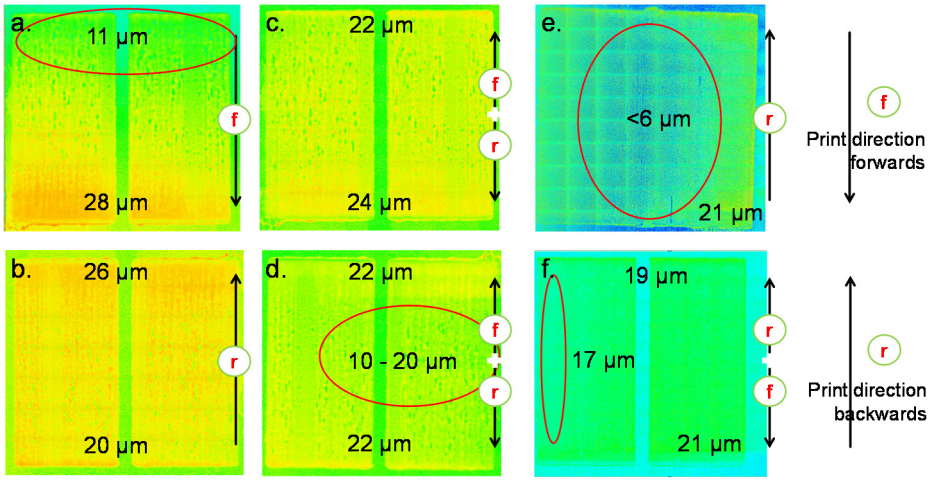


Figure 41: Printing characteristics of type 6 SnCn paste with 20 µm stencil for print velocities 35 mm/s; substrate SC $R_z \leq 16$ µm: a. 3.8 Kg, b. 3.0 Kg, c. 3.0 + 2.8 Kg, d. 3.0 + 3.0 Kg; substrate SPC $R_z \leq 5$ µm: e. 3.2 Kg (no bridge), f. 2.8 + 2.8 Kg.

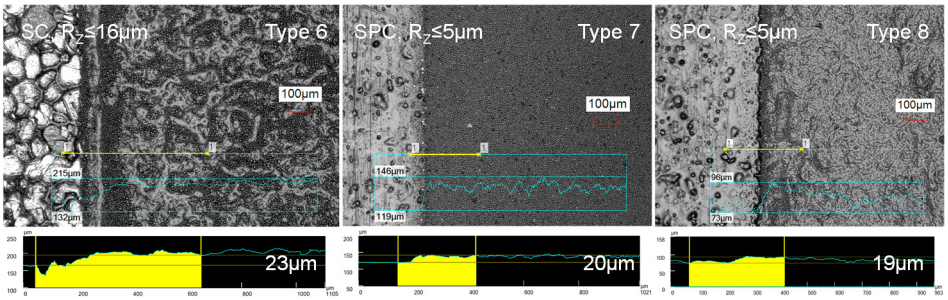


Figure 42: Microscopic images of printed solder paste types 6, 7, and 8 on DCB substrates of varying roughness.

The printing of type 7 and 8 solder pastes was also tested further to check the printability and height stability. The viscosity of the pastes increased with the type due to increased flux content for printability and solderability. For the selected parameters, the type 6 and 7 showed good printing characteristics, but the type 8 was relatively difficult due to very high viscosity irrespective of substrate roughness. Figure 42 shows the microscopic 3D-profile for the printed solder pastes with the above explained parameters. It can be observed that average paste height was near to 20 µm on the DCB substrates. Irrespective of the substrate roughness, the type 7 and 8 had homogenous surface profile due to small solder particles. For the tests with respect to the paste application for further experimentation, type 7 paste was considered in IMP formation and void formation.

5.2 Preparation for CAPM enhanced TLPS

The main goal for the integration of CAPM technology was to create thicker TLPS joints by depositing copper powder on the printed solder paste. The copper powder deposited reacts with the Sn from the solder paste forming IMPs during the thermal treatment and at the same time supporting the IMP formation from substrate side. In case of the composite solder approach from the HotPowCon project, even after extensive experimental analysis, a low-void interconnection with full IMP was not achievable under peak time of 4 min. This can be attributed to usage of copper particles sizes above 10 µm in the composite paste. A second reason can be that the required copper percentages of less than 38.7% in the interlayer. As explained in sub-chapter 3.1, for a 20 µm interlayer material, it takes by calculation, a thermal treatment of approx. 25 min at 260 °C for full transformation into IMPs. This is not practical as copper diffusion eventually slows down once the initial layers of Cu_6Sn_5 based on the critical interlayer thickness are formed. This needs a second source of copper particles other than from the copper substrate. This leads to the approach A2, that a homogeneous distribution of copper particles of small size in the solder deposit positively enhances the TLPS process in terms of diffusion distances and thus growth rates with it.

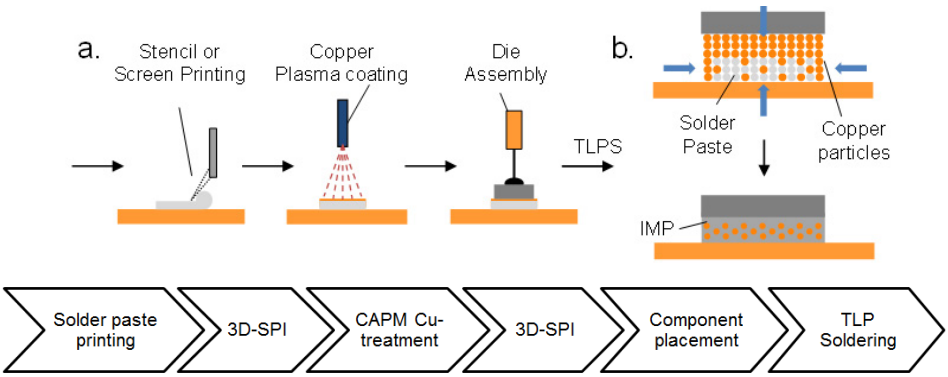


Figure 43: a. Procedure for Cu-plasmadust enhancement of the printed solder pastes. b. Strategy for the IMP formation for Cu-Sn system for solder paste.

The solder pastes $Sn_{99.3}Cu_{0.7}$ Type 6 and 7 were tested to analyze the printed copper particles and corresponding IMP formation. As test specimens, power electronic assemblies had been constructed by integrating the CAPM process step into the production line as shown in Figure 43, where the printed solder was treated with copper particles as inspected for interlayer height before and after the plasmadust treatment.

5.2.1 Considerations for the CAPM Treatment of Solder Deposits

The CAPM technology and its process parameters had been optimized for metallization of rigid substrates [167; 178; 179; 180; 181; 178]. But the application of Cu powder on solder paste without adversely disturbing the printed solder height and temperature-dependent material composition escalates the need for thoroughly refined process parameters. For checking the feasibility of the process integration and quality of the individual layers, the printed solder and consecutive Cu-plasma layers were inspected by a 3D-paste inspection system. Due to varying influential factors in the deposition process, an exploratory approach was preferred. The following points were considered in defining the spray parameters for reproducing the thickness of Cu layers deposited on the solder paste in the process window development:

- Variation of distance between the substrate and the plasma nozzle, until no solder layer was damaged through overheat or process pressure.
- Increase in number of cross-runs/ treatment steps
- Variation of powder quantity in plasma flow through disperser pressure and conveying gas flow
- Copper spray with and without plasma activation

The ultimate goal was to prevent the damage of solder paste height and paste volume during the process by the plasma gas pressure and temperatures. Further steps involved the building of thicker copper layers on multiple solder paste depots in the same step.

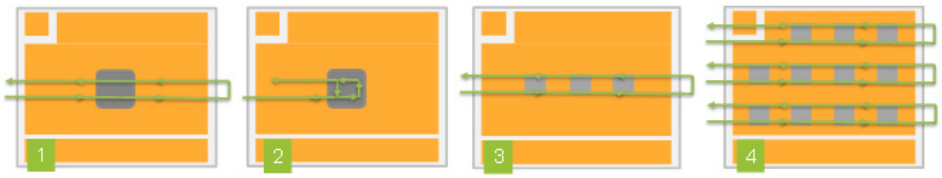


Figure 44: Test layouts and spray pattern for various component sizes used for the Cu-plasmadust treatment.

The optimized CAPM runs for different layouts are shown in Figure 44 and the obtained results from the integrated CAPM process are shown in Figure 45. It can be observed that a homogenous spray of copper was achieved on the solder deposits. For this purpose, a metal mask with a slight bigger pad dimensions was placed on the substrate with printed solder deposits during the CAPM process.

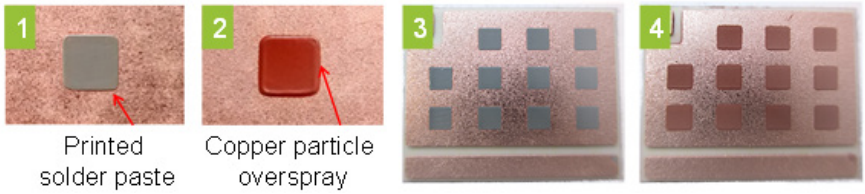


Figure 45: Produced specimens from the solder paste printing and Cu- plasmadust treatment for single component and multiple component layouts. 1,3: printed solder paste; 2,4. CAPM treated copper particles.

5.2.2 Influence of the Deposited Copper in IMP Formation

The DCB substrates were printed with Sn-Cu based solder paste with a 20 µm stencil and were treated with Plasmadust® to analyze the maximum possible copper coating. Upon initial tests with various deposition patterns, it was observed that the temperature of the test substrate increased to greater than 220 °C with increased plasma activated handling time, partly melting the solder material. To limit the temperatures to <180 °C, the deposition paths were modified accordingly. Figure 46 shows the double spray pattern with plasma activation (Strategy 1: S1), where the copper particles were partially melted and fused during the spray step. The increase of substrate temperature during each layer deposition required cooling of the substrate even with increased substrate-nozzle distance. Figure 46 shows the variants considered, copper application strategies and resultant coated depot height in consecutive spray steps. Therefore two process windows had been designed for the two explained strategies summarized in Table 15. It can be observed from Figure 46, that the consecutive layers deposited with S1 showed very fine surface texture compared to S2. Figure 46 shows also the slight path planning of circular spray pattern without plasma activation (Strategy 2: S2), resulting in precise deposition of dry unmelted copper powder with controllable layer thickness. The main problem for obtaining reproducible results for this present concept was the inadequate process stability. In both cases, the possible coating thickness reached a maximum as seen in depicted curves at approx. 39 µm and 76 µm for S1 and S2 respectively. It was observed in S1 that with increased deposited amount of Cu on the solder, fewer particles adhered to the previously deposited layers even upon increased process pressure. This effect occurred also by S2 but much later, can be attributed to the fact that the installed gas stream upon activation of the system without plasma flame was under 20 l/min. The pressure upstream of the nozzle was thus significantly lower resulting in deposition of thicker layers.

Table 15: Overview of the plasmadust parameters used for strategies S1 and S2

Process parameters	**Nozzle distance (mm)**	**Substrate velocity (mm/s)**	**Disperser pressure (bar)**	**Gas flow (l/min)**
Standard [182]	8 – 12	50 - 150	1.2	45
Strategy 1 (S1)	35 – 40	25 – 35	1.5	35
Strategy 2 (S2)	30 – 35	5 – 10	1.5	35

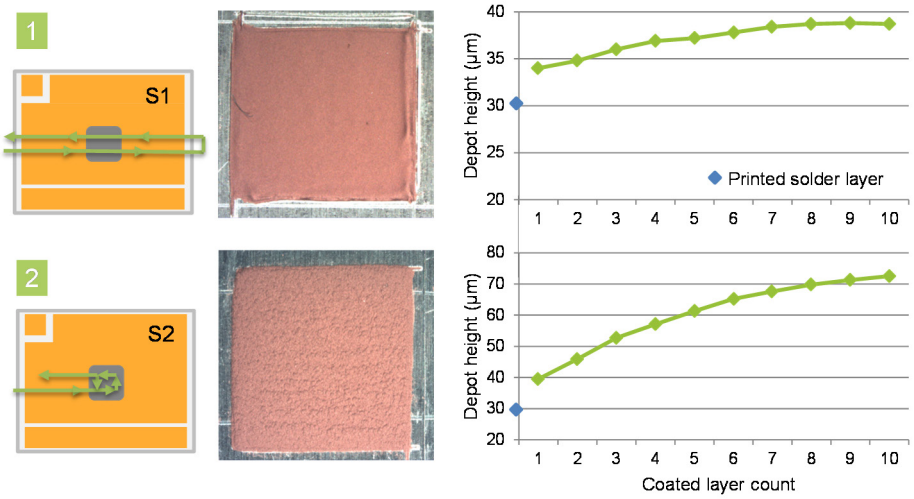


Figure 46: Depot surface and height growth of different application methods with plasma activation [Strategy S1, 1] and without plasma activation [Strategy S2, 2].

How deep the copper particles were spread into the solder depot during the initial sprayed layers was extremely difficult to analyze. Increased powder thickness led to soldering problems with no proper melting or non-wetting of particles. This is due to the insufficiency of flux solvent inside the printed solder paste for activation of abundant copper material. It must also be considered that for a proper wetting of particles and fusing with the solder melt, the particles must be properly dispersed into the solder layers. As discussed earlier, the depth of the penetration into the fluidic solder during plasma process is extremely difficult due to high pressure speeds and gas pressures. This was possible with plasma activated CAPM process of strategy S1 but with lower gas flow rate and increased nozzle distance to avoid the flux burnout or solder melt problems during the CAPM.

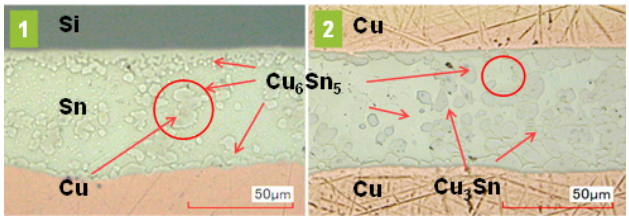


Figure 47: Initial results of interconnections realized by the plasma enhanced solder interlayers for Ni-Ag metallized silicon semiconductor components (1) and Cu metallized bronze components (2).

The modules were built from components with standard NiAg and Cu metallizations on bare DCB substrates. Figure 47 shows the cross-sectional images of produced standard solder joints as a reference. For a 80 µm printed solder layer with 10 µm coated copper powder with plasma activation (S1) (similar to chip copper backside metallization) and standard VVP profile (peak temperature 250 °C for 90 sec), it can be observed that the initial IMPs were formed at the component side and also in the middle of solder layer from the penetrated copper powder into the solder interlayer. But for the copper metallized components, the IMPs were thicker due to diffusion of Cu from metallization of the component. A scallopial structure in case of silicon component could not be observed in comparison with Cu-metallized component. Further investigations in the IMP analysis and defects are explained in sub-chapter 7.2.

5.3 Preparation and Placement of TLPS Enhanced Preforms

The solder preforms allow customized product developments and faster product design with greater flexibility. Though presently the production and usage of solder pastes is dominant compared to solder preforms, the trend shows the usage of preforms to increase the production flexibility and automation significantly. For the approaches B1 and B2 for the TLPS process, the new die-attach preforms were investigated at FAPS on the feasibility and developed together with company 'Pfarr Stanztechnik GmbH'. These developed TLPS preforms were purely lead-free alloys and can be fluxless soldered under 280 °C. The tested substrates here in this case were the variants SPC and SNC with $R_z \leq 5$ µm. Even in the case of preform-based fluxless soldering, the usage of the preform-thickness less than 80 µm is avoided due to various handling issues during placement process and corresponding solder defects. Initially as part of this thesis work, fluxless

solder preforms of thickness 25 µm were tested with respect to the compatibility and voiding characteristics. The tests with CFL soldering showed that the temperature profiles were not efficient as in case of conventional 100 to 200 µm fluxless preforms. This needed optimization with respect to voiding similar to thin solder layer thicknesses. As part of thesis, both the conventional and newly developed alloys which are suitable for different types of substrates and metallization were tested and the solder profiles were optimized. The preform materials include Sn-Cu bimetallic systems and one variant with Ni additive for nickel metallized substrates. The thickness of the tested alloys for TLPS ranged from 25 µm to 30 µm for approach B1. However the thin preforms had complications with respect to handling with placement systems and had to be placed manually. To increase the flexibility with preform handling, thicker preforms were developed at thickness between 75 µm and 85 µm for approach B2.

Table 16: Overview of the developed preform compositions and their thicknesses.

Approach	Preform name	Composition	Thickness (µm)
B1	B1P1	$SnCu_{3.0}$	22.5 ± 2.5
B1	B1P2	SnCu2.9Ni0.05	22.5 ± 2.5
B2	B2PC	Sn-Cu-Sn Cladded	25 - 30 - 25

The production of the preforms mainly followed the steps of alloying of the materials followed by rolling into sheets of appropriate thickness. The rolled sheets of the alloys were stamped or slitted according to the required shape in the application. In the case of preparation for thin preforms, high quality of the rolling equipment was required. For the approach B1 and B2, the preform variants developed and used as part of the work are given in Table 16. The total combinations of additives did not exceed 3% of the total composition to ensure good wetting to substrates.

Modification of preform structure for TLPS with thicker bondlines

For the thin preforms of 25 µm, the TLPS profile developed for solder pastes worked with high reproducibility. However for thicker preforms of same alloy type, a modification of solder profiles is not really feasible with large scale production due to prolonged process time for full IMP formation of more than 50 µm in the bondline. The structure of the preform was modified as cladded version of thin copper and tin foils.

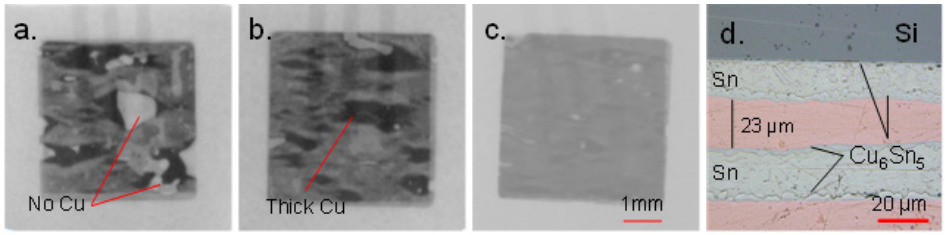


Figure 48: X-ray images of the cladded preforms soldered with silicon semiconductor chips: a. defective, b. uneven and thicker Cu, c. homogenous Cu, d. cross-section of the cladded preform soldered with peak time of 2.5 min.

The cladded preforms were fabricated in range of 70-80 µm thickness similar to the normal preforms however rolled as stacked sheets before slitting. This however showed some variations in the final copper and tin thicknesses in the final preform structure as showed in Figure 48. In less than 5% of the cladded preforms, uneven distribution of copper was observed as in Figure 48.a,b. The preforms though had few defects, were evenly filled with tin material. A homogenous distribution of the copper in the preform and a cross-section can be seen in Figure 48.c. The goal was to improve the preform handling during the placement in assembly process. An advantage here is the flexible modification of copper layer thickness. The top layer and bottom Sn had approx. 20 µm thicknesses and Cu of 30-40 µm respectively. The tests were performed on both SPC and SNC DCB variants. A cross-section of the soldered structure on SPC substrate is shown in Figure 48.d.

5.4 Conclusion

In this chapter, initially the stencil printing of thin solder layers down to 20 µm was introduced. The obtained paste height and the paste volume were highly dependent on the chosen paste type and substrate roughness. For the substrates SC with roughness of $R_z \leq$ 16 µm, paste type 7 and type 8 showed average paste heights of 19 µm. For SPC of $R_z \leq$ 6 µm, the same pastes and printing parameters showed average of 24 µm solder height. This can be attributed to the compatibility of particle sizes with the substrate roughness. For further testing with TLPS process, the paste type 7 was considered as the first priority due to homogenous paste application even for larger pad dimensions. Solder paste type 6 however resulted in scooping effect or scratch effects on smoother surfaces due to improper rolling of particles during paste deposition.

From section 5.1, the following conclusions can be interpreted:

- The solder paste $SnCu_{0.7}$ was considered instead of SAC solder for the TLPS process development and optimization.
- Ag_3Sn IMP hindered the formation of Cu_6Sn_5 IMP in SAC solder pastes.
- For procuring solder deposits as thin as 20 µm, solder paste with particle sizes of type 6 or lower was required.
- Printing experiments resulted in reproducible paste volumes and uniform paste distribution in case of type 6 and type 7 solder pastes.
- A stable printing parameter combination was finalized for the printing of solder pastes with thin stencil down to 20 µm.
- Squeezee pressure was mainly varied to obtain a stable process window keeping the print velocity constant.
- Type 8 solder paste though had a good printability resulted in print defects with respect to unstable paste flow under the stencil out of apertures.

For the CAPM-based TLPS approach, a uniform and a thin powder layer of maximum 15 µm on paste height of 90 µm was deposited. This was done with multi-paths of at least six plasma runs to allow the sufficient penetration of copper particles into solder deposit followed by the copper powder layer completely covering the solder deposits. From section 5.2, the following can be concluded:

- A uniform copper powder layer on the solder deposit was possible with modified parameters of the CAPM process.
- The strategy with plasma activation resulted in better and controllable copper powder thickness on the solder deposit.
- Though the penetration of copper particles into the solder paste cannot be quantified, the soldered assemblies showed increased IMP formation com-pared to normal solder deposits.
- Due to the deposited copper, Cu_6Sn_5 IMP clusters were observed along with scallopial IMP formation at the component boundaries.

The interlayer materials i.e. cladded structures in case of B2PC preforms and compositions in case of B1P1 and B1P2 (with Ni additive) which are used for investigations in the feasibility of the preform-based TLPS were also introduced. The thin-preforms were placed manually, but the thicker preforms were handled without effort increased highly the flexibility with the placement machines.

The following can be concluded from all the investigations in this chapter:

- The printing of solder pastes down to 20 µm helps in easier IMP formation, as lower process time is possible to transform the tin in solder into IMPs.
- The abundance of flux material in solder may lead to increased void formation worsening the joint quality.
- Copper powder deposition i.e. increase of copper content in interlayer not only increases the process flexibility, but also reduces the process time.
- The preform materials compared to the paste based approach allow reduction of total costs in materials and maintenance.
- Usage of preforms shortens also the process chain and increase the handling flexibility and customization.

6 Investigations for a Void-free TLPS Process

In this chapter, the results of the simulations performed for estimating the time required for a successful diffusion are explained primarily. Here various test profiles were imported from the developed 'temperature profile generator' to 'concentration-gradient based simulator' to estimate the influences of the pre-heating holding time, peak time and post-handling time. Depending on the obtained required time from simulation for full IMP formation for specific interlayer height, the preliminary tests were conducted to mainly evaluate the IMP formation and verify the simulation results. Further analysis was performed mainly in the voiding analysis to observe the resulting void percentages due to reduced thickness of the interlayer, increased peak time and increasing component size without use of any void-reduction techniques. These tests and results were considered as a prerequisite for further modification of temperature profiles. In this chapter, also the primary investigations with void-reduction mechanisms mainly vacuum and over-pressure are also summarized. These are supported by the in-situ investigations performed for the solder joints. A brief summary is given on the observed process generated defects and optimization measures are discussed.

6.1 Simulation of Diffusion Process and Case Study Analysis

A statistical estimation on the amount of time needed for a total transformation of IMPs in the bondline by experimentation is relatively difficult due to various influential factors and time consuming individual process steps. However, a simulation of the diffusion process would give an approximate estimation on the time on the interdiffusion length. For this, a concentration gradient based computational domain simulation [183] was performed for the simulation of the IMP formation in the interlayer for a simplified bimetallic model. The software Comsol Multiphysics [122] was used in combination with MATLAB to derive simulatively the time needed for the IMP thickness and diffusional variation in the Cu-Sn system through the atomic concentration changes. The surface roughness of the individual material domains is zero and no thermal convection or pressure influence is assumed for the part of the simulation.

Model setup and boundary definition

A simple 2D model of copper and tin each of thickness 40 µm and 3 mm in length was defined in Comsol 'geometry module' to reduce the computational complexity and time. The model was dimensioned at mesh elements of 0.1 µm (x) and 0.2 µm (y). In the Figure 49, the representation is vertical however the original simulated computation was horizontal. Here, flux boundary conditions are crucial particularly for the design of concentration simulation of an inter-diffusion scheme where heat transfer and diffusion simulations are coupled by flux exchange algorithms. For these schemes to be conservative the flux leaving one system must enter the other.

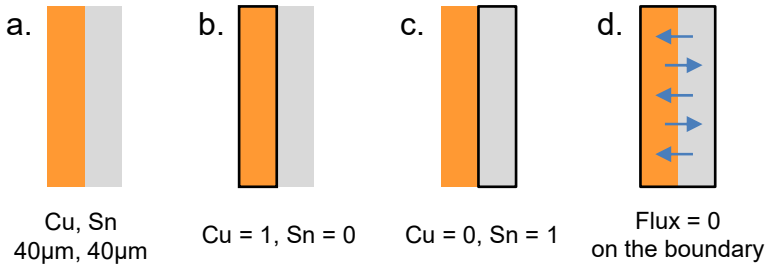


Figure 49: Initial condition at the domain (a) defined thickness of Cu and Sn zones (b) Cu=1, Sn=0, (c) Cu=0, Sn=1 and boundary condition (d) flux=0 at the edge.

During IMP formation, inter-diffusion which is driven by atomic concentration gradient can be described by the Fick's second law [184] as explained in sub-chapter 3.1. Initially the reaction is assumed to be zero at the interface. So the transport of diluted species module as introduced in sub-chapter 4.3 is defined according to this assumption. This module follows the generic diffusion equation which has the same structure as the heat conduction equation and is governed by the following mass transfer equation (6). As the convection is assumed to be zero, the equation (6) for the concentration 'C' is prepared according to the assumption.

$$\frac{\delta C}{\delta t} + \left(D \frac{\delta^2 C}{\delta x^2} \right) = G \qquad (6)$$

Where G is the reaction rate. For the simplicity of the model, reaction rate will be assumed to be zero here (G=0), then the equation (6) would be in below form.

$$\frac{\partial C}{\partial t} + \left(D \frac{\delta^2 C}{\delta x^2} \right) = 0 \tag{7}$$

Equation (7) is the governing transport equation for the diffusion soldering process. Where D is the growth rate constant which is equivalent to diffusivity as the IMP formation in the TLPS is diffusion controlled.

According to the Arrhenius equation (8) in agreement with equation 5 from sub-chapter 3.2 as below, the diffusivity is determined by the activation energy Q *(KJ/mol)*, the diffusion coefficient D_o *(m^2/s)*, and the absolute temperature T *(K)*.

$$D = D_0 exp\left(-\frac{Q}{RT} \right) \tag{8}$$

Where *R (J/(mol×K)* is the universal molar gas constant. The universal gas is composed by Boltzmann constant and Avogadro's Constant. So the value of *R* can be calculated by multiplying Boltzmann constant with Avogadro's constant where the

Boltzmann constant = $1.38064852 \times 10^{-23}$ m^2 kg s^{-2} K^{-1} and Avogadro's Constant = 6.02214086×1023 mol^{-1}.

As part of this simulation, the concentrations were considered as in Figure 49. Initial condition was selected as 100% Cu and 0% Sn in left computational domain and 100% Sn and 0% Cu was selected in the right computational domain. 'No flux' boundary condition is implemented at the outer boundary of the computational domain. One of the important inputs for the simulation is the boundary conditions at the interface between two reacting media [122; 183]. At the boundary, two conditions are mainly specified.

1. A condition that links the inter-dependent variable in the two regions
2. A condition that links the flux of the dependent variable in each region

The continuity of the flux across the boundary between the sub-computational domains and also the continuity of the dependent variable are the important considerations. Here the local boundary conditions that allows the fluxes of momentum and energy are simultaneously specified either as free parameters or in order to simulate an external parameter.

Procedure for simulation and evaluation of generated concentrations

The simulation methodology is mainly divided into three stages using Comsol and MATLAB as shown in Figure 50. The developed script 'temperature profile generator' generates the user defined temperature profile over the time for three predefined time-temperature models as shown in Figure 51. The Comsol module *'transport of dilute species (tds)'* imports the generated temperature profile as a global function for the computational domain of Cu-Sn system. Only transport phenomena of the species are computed here and reactions are assumed to be zero. The driving force for the transportation is diffusion which is expressed by Fick's law.

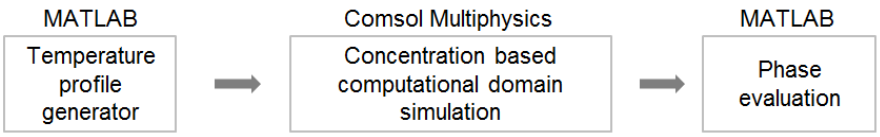


Figure 50: Simulation overview process for the softwares Comsol and Matlab.

The computational domain of the Cu-Sn model is predefined with parameters mainly the activation energies and diffusion coefficients for the mass transportation equations. The concentration gradients simulated in each of the sub-computational domain over time are exported into MATLAB. In the developed script, the concentration values in the vertical length are evaluated on the IMP formed in each of the domains. For the analysis of the IMPs for the imported thermal profiles, the simulations were run for each variation in form of individual case studies for peak temperatures of 260 °C and 280 °C with varying peak times and thermal treatment. The heating and cooling gradients of profiles were varied from 0.5 K/s to 3 K/s.

6.1.1 Profile Generator for Transient Thermal Input

The COMSOL setup of Cu-Sn system is fed with a transient temperature profile with following parameter variation as tabulated according to the profile model type in Table 17. The main defined parameters in the profile generator were initial temperature (T_i) i.e. room temperature, heating gradient (Δ_H), cooling gradient (Δ_C), handling time (t_h), intermediate temperature (T_{inter}) and intermediate handling/ annealing time (t_a). The case study analysis performed for the results of the simulation is summarized in the sub-chapter 6.1.3. The comparison of the preliminary investigations and simulation results for verification is explained in sub-chapter 6.2.1. As the TLPS process depends on diffusion between solder and substrate, the

concentration changes in Cu-Sn system mainly depend on temperature dependent diffusion coefficients. As the temperature changes, the diffusion coefficient of both Sn and Cu were taken as time dependent global variables during the simulation. The goal behind choosing varying handling temperature and times was to estimate the phase formation with outlook to low void percentages. The advantages of the post-handling at lower temperatures with respect to the void percentages are discussed in sub-chapter 7.1. The generated profiles with Matlab are also displayed in Figure 51. The main difference between model 1 and model 3 are thermal treatment temperatures at 260 °C and 210 °C respectively. The model 2 however mimics a plateau profile in standard soldering machines with extended profile times.

Table 17: Overview of the profiles generated and used for the simulation.

Simulation models	**Model 1**	**Model 2**	**Model 3**
Peak temperatures (°C) [T_P]	260, 280	260	260
Initial temperature (°C) [T_i]	-	210 (pre)	210 (post)
Peak handling time (min) [t_P]	1.5, 5 to 30 in steps of 5	5, 10	1.5, 5, 10
Intermediate handling / annealing time (min) [t_a]	-	5, 10	5 to 30 in steps of 5
Heating gradients (K/s) [Δ_H]	0.5 to 2.5	2.5	2.5
Cooling gradients (K/s) [Δ_C]		2.5	2.5
Case study number	1, 2, 3, 4	5	5, 6

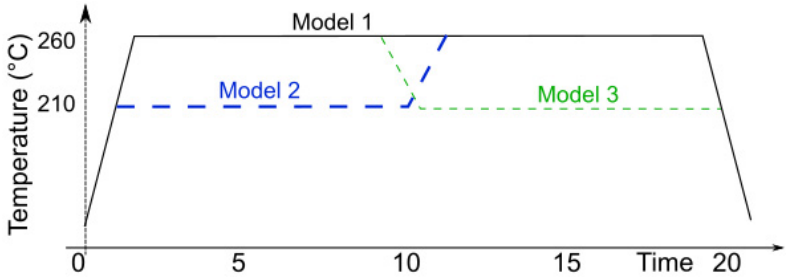


Figure 51: Generated temperature profiles as input to COMSOL for Model 1: 260°C, Model 2: 210°C, 260°C; Model 3: 260°C, 210°C as in Table 17.

6.1.2 Results of the Concentration Gradient Simulation

The finite element model shows how copper diffuses into tin atomic structure and vice versa. The Figure 52 illustrates the location of Sn and Cu atoms in the computational domain. In the figure dark red area defines the atomic concentration of Sn and on the other side blue color represents copper. At the beginning of the simulation (t=0), there was no diffusional variation, hence no concentration changes in between Cu and Sn. During and after the simulation, the concentration gradients vary according to the temperature profile input and time as shown below.

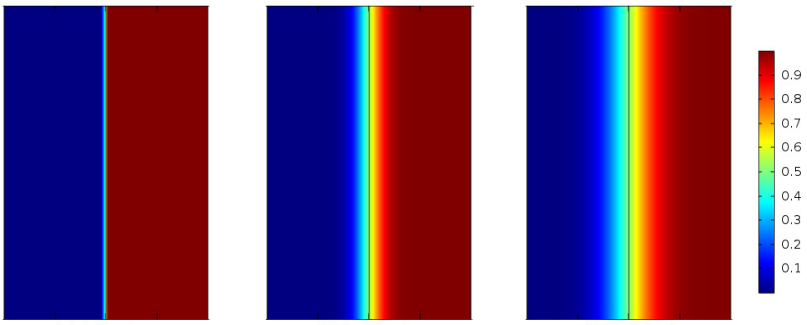


Figure 52: Normalized atomic concentration changes with Cu | Sn at (a) t=0 min, (b) t=10 min, (c) t=30 min; scale for Sn = 0 to 1 normalized.

Figure 52 also shows how the variation can be observed at each of the interfaces with varying concentration. At t = 0, 10, and 30 min, the diffusion length of bimetal system changes according to the input peak time. The output from the simulation is the atomic concentration of Cu-Sn system with respect to the location and time. The results were analyzed in MATLAB for concentration data generated from COMSOL in computational domain are shown in the Figure 53. This shows the 280 °C peak profile (Model 1) for t_p = 30 min for the materials pure Cu, Cu_3Sn (ε) Cu_6Sn_5 (η) and pure Sn respectively. The atomic concentration profile is plotted along the perpendicular direction of IMC interface at the time coordinates. At the end of total simulation for the profile of approx. 33 min, a Cu_6Sn_5 phase of 11.9 µm and Cu_3Sn phase of 1.9 µm were obtained. The same is shown on the right where both IMP formations (i .e. Cu_6Sn_5 and Cu_3Sn respectively) are represented for the input temperature and time profile for T_P of 280 °C.

For a specified input profile, e.g. after 30 min, the concentration of the system doesn't change as it arrives to an equilibrium. Further the tin and copper concentration doesn't change over time. As in this simulation reaction, the physical influential factors like pressure or atmosphere are

assumed to be zero, after equilibrium, the concentration gradient is zero. But if the influential parameters (e.g. chemical reactions with flux, pressure or energy transfer type) are taken into account, the equilibrium point will adapt giving a more realistic result.

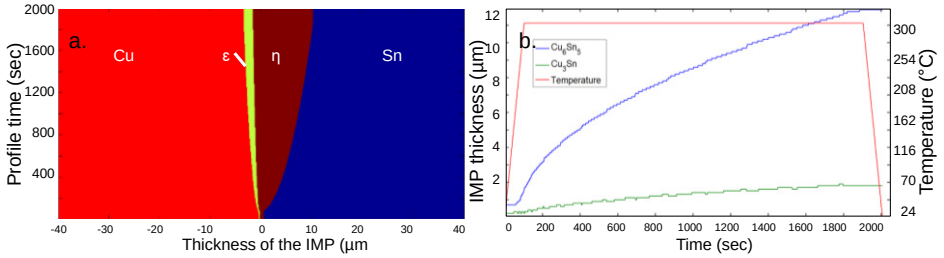


Figure 53: a. Thickness of IMP formation over time; b. IMP thickness according to the temperature profile for peak temperature of 280 °C.

Figure 54 shows the simulation results for the phase evaluation over the time at peak temperature of 260 °C and 280 °C with the peak time 't_P' of 5 min and 30 min. The result of η-IMPs for 260 °C profile was 4.3 µm and 9.9 µm and ε-phase of 0.7 µm and 1.6 µm respectively. This also shows that the diffusion kinetics varies from the 280 °C profile as shown in same figure as comparison.

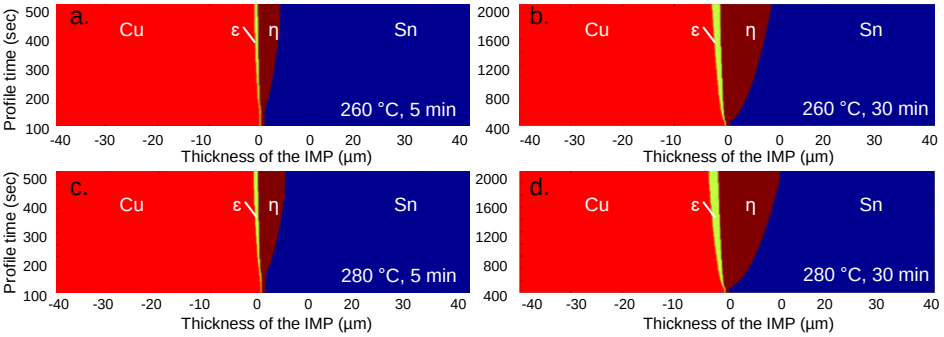


Figure 54: IMP evaluation over time at peak temperature at 260 °C: a. t =5 min, b. t =30 min; at peak temperature 280 °C: c. t =5 min, d. t =30 min.

6.1.3 Case Study Simulation for the IMP Estimation

After having the result from the developed simulation method, simulations with varying parameters were performed to understand the influences of the low-temperature pre- or post-thermal handling of the Cu-Sn system. These were mainly the variation for peak temperature (T_p), peak handling

time (t_P), annealing time (t_a), heating gradients (Δ_H) and cooling gradients (Δ_C) as explained in Table 17.

Case study 1 & 2: Influence of peak handling time t_P and peak temperature T_P

In this case study, heating (Δ_H) and cooling (Δ_C) gradients were set to 2.5 K/s. For T_P of 260 °C and 280 °C, the handling time (t_h) was varied from 1.5 min to 30 min. The total time of the longer profile was 33 min including heating and cooling. The handling time tP of 1.5 min represents the conventional reflow solder profile.

It can be clearly observed from the Figure 55, that the temperature and time both have a proportional influence and linear behavior on both the η- and ε-IMP formations. However, the influence on the η-phase is significantly higher due to lower activation energy. The ε-IMP had low influence irrespective of peak temperatures i.e. 260 or 280 °C, due to higher activation energies and generally is formed at higher temperatures as part of solid-solid interdiffusion. The resultant thickness for the η-IMP is comparatively higher for 280 °C as explained above. The temperatures of 260 °C, which are close to the conventional soldering, a η-thickness of 9.9 µm is obtained for 33 min profile. In this simulation, as the diffusion is mainly at the interface of tin and copper. It can be inferred that a presence of abundant copper on both sides of tin with peak handling time of atleast 30min at 260 °C, a η-IMP thickness of ~20 µm is realizable. Based on this, further experimentation was performed for solder profiles upto 30 min with variation in solder layer thickness with and without copper availability for diffusion.

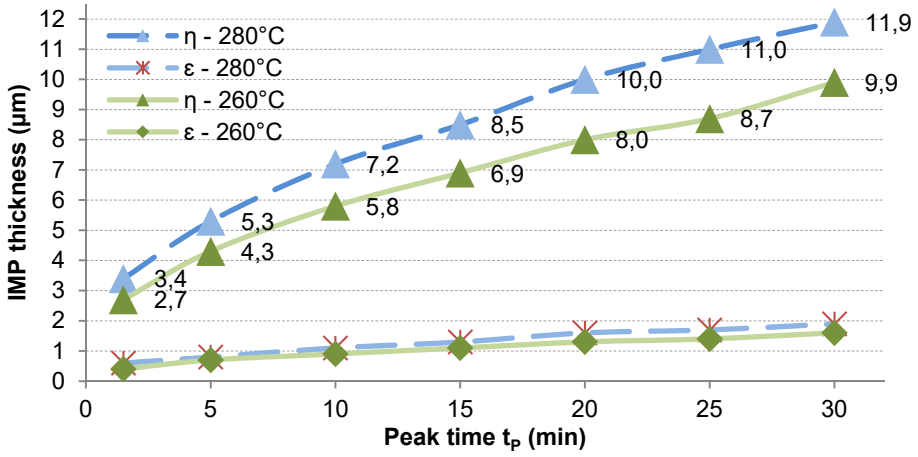


Figure 55: IMC growth over handling time (t_h) at Tp= 260 °C and 280 °C with fixed $\Delta_H = \Delta_C$ = 2.5 K/s.

Case study 3 & 4: Influence of the heating Δ_H and cooling gradients Δ_C

In these case studies, the thermal inputs were varied with heating and cooling gradients for T_P of 260 °C for peak handling times t_P of 1.5, 5 and 10 min. For case study 3, Δ_H was varied from 0.5 to 3 K/s and Δ_C was set constant at 2.5 K/s. The opposite was tested for case study 4, with Δ_H set at 2.5 K/s and Δ_C varied from 0.5 to 3 K/s. It can be observed that the variation of the heating gradients had a noticeable variation in the η-phase formation, which can be explained due to the increased energy transfer with decreasing heating gradient, i.e. longer time at a specific temperature. The cooling gradients however had no noticeable variation, as it is a pure theoretical simulation, a slight decreasing effect was seen which is generally not true in case of actual solder behavior. Practically the cooling gradients have an influence on the thickness of IMPs. For example slowly cooled assemblies are observed with slight higher Cu_6Sn_5 growth compared to faster cooling gradients i.e. assemblies cooled rapidly through water or forced air.

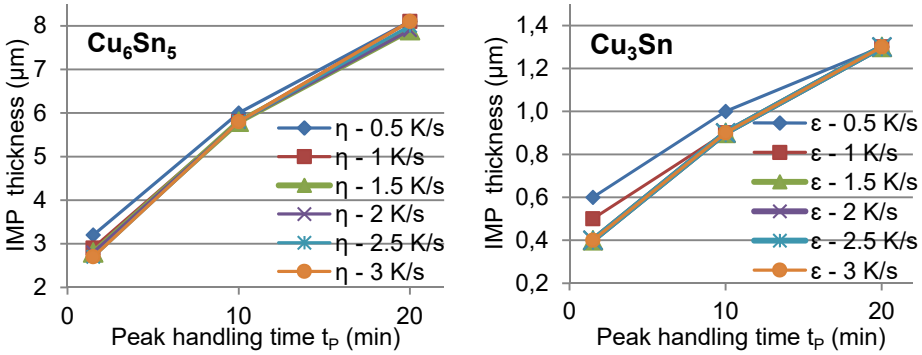


Figure 56: IMC growth of Cu_6Sn_5 and Cu_3Sn over handling time (t_h) for various Δ_H, for T_p= 260 °C, Δ_C = 2.5K/s.

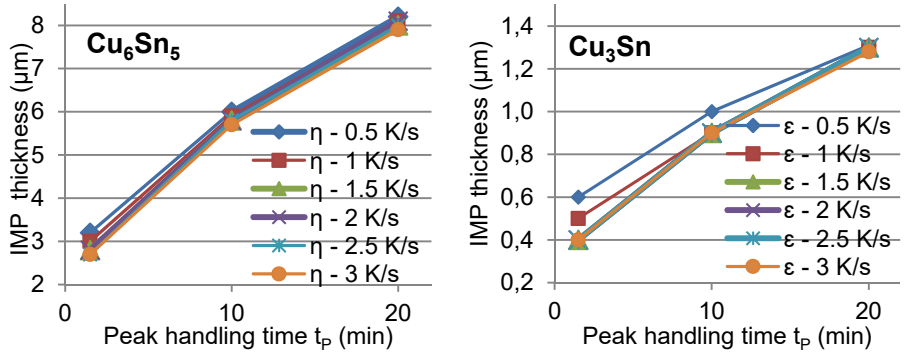


Figure 57: IMC growth of Cu_6Sn_5 and Cu_3Sn over handling time (t_h) for various Δ_C, for T_p= 260 °C, Δ_H = 2.5K/s

Case study 5: Influence of thermal pre-handling and post-handling time t_a

Apart from the peak temperature handling, the IMP formation due to the pre-handling and post-handling was simulated. The main reason for this case study was due to generation of process related defects upon prolonged peak temperatures. Though an additional pre-handling or post-handling step with reduced peak temperature time might produce lower IMP in the model, a significant improvement in the process quality was observed during experimentation. This is explained further in the next chapter. For this case study, the profile models 2 and 3 as explained in Figure 51 and Table 18 are considered. Here the heating and cooling gradients were kept constant at 2.5 K/s, but the time for peak and pre-/ post-handling temperatures are modified as in Table 18 below. It can be observed that irrespective of the thermal handling considered, the values are relatively similar in case of simulations which are directly dependent on the temperature and the handled time. The void analysis and the obtained IMP thicknesses for these profiles are explained in sub-chapter 7.1.

Table 18: Overview of used parameters and obtained IMP simulation results for study 5.

Model 2 profile				Model 3 profile			
Pre-handling time at **210 °C** [min]	**Peak** holding time at **260 °C** [min]	Avg. η (Cu_6Sn_5) IMP [µm]	Avg. ε (Cu_3Sn) IMP [µm]	**Peak** holding time at **260 °C** [min]	**Post**-handling time at **210 °C** [min]	Avg. η (Cu_6Sn_5) IMP [µm]	Avg. ε (Cu_3Sn) IMP [µm]
10	10	6.46	0.94	10	10	6.48	0.93
10	5	5.1	0.79	10	5	6.31	1.0
5	10	6.24	0.98	5	10	5.2	0.8

Case study 6: Influence of the peak t_P and post-handling time t_a

Generally, the void percentages obtained in the conventional soldering interconnections are influenced by numerous parameters where the outgassing of the flux materials and peak handling time of solder material play a major role. A thermal treatment of peak temperature of 260 °C for 30 min compared to 10 min had a significant difference in the void percentages. However in this case study, mainly the goal was to check the IMP formation

for varying post-handling time for fully transformed η-phase in the bondline. It can be observed from the simulation IMP values that with a t_P of 5 min at 260 °C and t_a of 30 min at 210 °C or with t_P of 10 min and t_a of 15 min, the same amount of η-IMP thickness of 6.8 µm can be obtained as in Figure 58. This also shows that t_P of 1.5 min at 260 °C and t_a of 30 min at 210 °C or with t_P of 5 min and t_a of 15 min, the same amount of η-IMP thickness of 5.6 µm can be obtained. This gives a clear overview of how the profiles can be modified according to the requirements. For the ε-phase, the requirement is similar to electronics production, i.e. possibly low thickness in the resultant bondline.

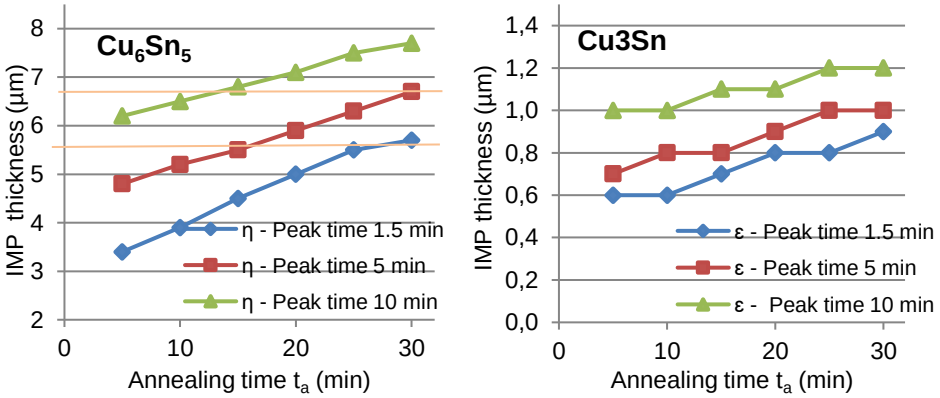


Figure 58: IMC growth of Cu_6Sn_5 and Cu_3Sn over annealing time (t_a) for various peak time t_P for T_p= 260 °C, T_i= 210 °C, $\Delta_H = \Delta_C$= 2.5 K/s.

6.2 Preliminary tests for IMP formation in TLPS process

Based on the preliminary simulation values, the main objective of the conducted experiments was to check the thickness of produced IMPs according to the temperature profiles on the bare copper substrates. Here for the tests, no any components were placed on the solder material. The variation was also the roughness of the selected DCB substrate materials (SC of $R_z \leq$ 16 µm and SPC of $R_z \leq$ 6 µm) as described in section 4.3. The tested profiles as shown in Table 19 were with peak temperature T_p of 260 °C and heating gradient Δ_H of 2.5 K/s. The temperatures corresponding to the T_p and T_a were the measured temperatures directly on the surface of the substrates with thermo-elements.

Table 19: Overview of the tested temperature profiles

	Test model 1	**Test model 2**	**Test model 3**
Peak temperature (T_p) [°C]	260	260	260
Annealing temperature (T_a) [°C]	-	210 (pre)	210 (post)
Peak handling time (t_P) [min]	5, 15, 25	20	10
Intermediate handling/ annealing time (t_a) [min]	-	5	15
Heating gradients (Δ_H) [K/s]	2.5	2.5	2.5
Profile names	**P1, P2, P3**	**P4**	**P5**

For these experiments, the solder paste material $Sn_{99.3}Cu_{0.7}$ of Type 6 and flux material F645 was used. The paste was applied at paste thickness of 60 µm using stencil printing on both substrate variants for each profile combination. The temperature profiles were run on a reworking station with precise control of the parameters. The heating mechanism was heat conduction from the base platform in the rework station. The specimens were then evaluated for the Cu_6Sn_5 and Cu_3Sn IMP thicknesses. The evaluation was performed by cross-sectional analysis and measurement of both the phases to arrive at a statistical conclusion. The IMPs thicknesses were measured at at least 8 positions in each cross section of every specimen. The average thicknesses of both IMPs are shown in Figure 59.

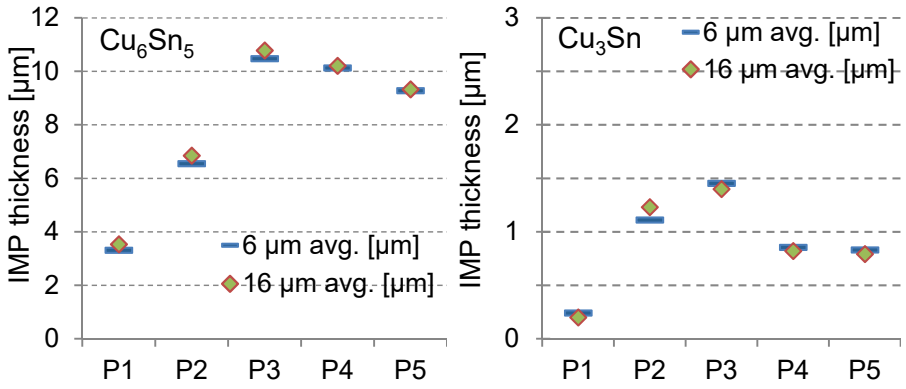


Figure 59: Thickness of Cu_6Sn_5 and Cu_3Sn IMPs for test profiles as in Table 19.

It can be observed that the average η-phase thickness is evidently higher for profile P3 of higher peak handling time of 25 min. It can also be observed that the thickness is slightly higher for substrates SC of higher roughness.

The thickness of ε-phase however did not show much dependence on the roughness as the layer formed was comparatively thin. The profiles P4 and P5 with pre-handling or post-handling had comparatively low IMP formation with full peak time handling of 15 min. The investigations with respect to the profiles P4 and P5 though produced lower IMP thicknesses, were to check the influence on the voiding characteristics which are explained further in section 7.3.

6.2.1 Comparison of Experimental Results with Simulation

In this section, comparison between the obtained of Cu_6Sn_5 and Cu_3Sn IMP thickness values from the experiments and simulations are compared. The comparisons are performed mainly for the temperature profiles with peak temperature of 260 °C and 280 °C with varying handling time. For the experiments, the heating and cooling gradients (Δ_H, Δ_C) were set to 2.5 K/s. As it can be observed from the Figure 60, a handling time of 30 min of 260 °C produced an average η-IMP thickness of 12.1 µm. The actual IMP thickness depends on the amount of the copper available at the point of time from the substrate. The values η and ε-IMPs for conventional soldering profiles with tP of 90 sec are obtained accurately at 2.5 µm and 0.1 µm respectively.

Figure 60 shows the influence of the surface roughness in the IMP formation. In case of smoother surfaces, the IMP growth was relatively flat parallel to substrate surface. But the IMP growth on the rougher surface mimics the surface profile as also explained in chapter 5. Figure 60 shows the cross-sectional images of the test samples with varying peak time. It can be observed that the growth of the IMP increases with the peak time.

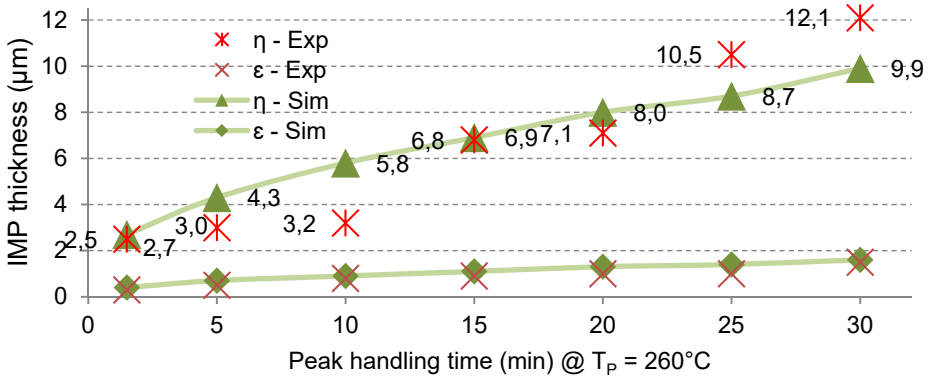


Figure 60: IMC growth comparison of experimental and simulated Cu_6Sn_5 and Cu_3Sn phases over handling time (t_h) where, T_p= 260 °C, $\Delta_H = \Delta_C$= 2.5 K/s.

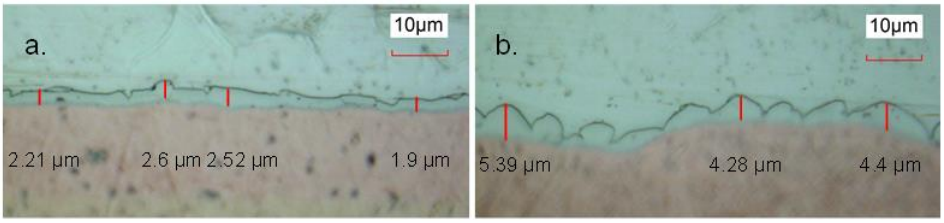


Figure 61: Influence of surface roughness on η-Cu_6Sn_5 formation for: a. SPC at T_P = 260 °C, t_P = 2.5 min; b. SC at T_P = 280 °C, t_P = 10 min.

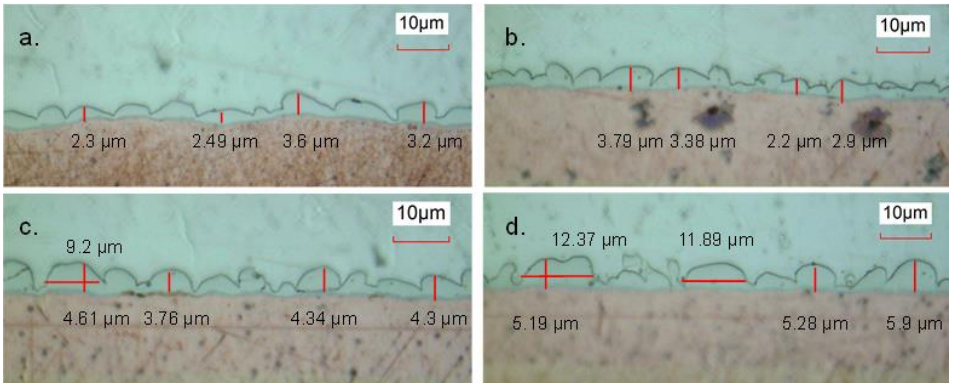


Figure 62: Influence of peak time on η-Cu_6Sn_5 formation on SC substrate for T_P = 260 °C, t_P: a. = 2.5 min; b. = 5 min; c: = 10 min; d = 15 min.

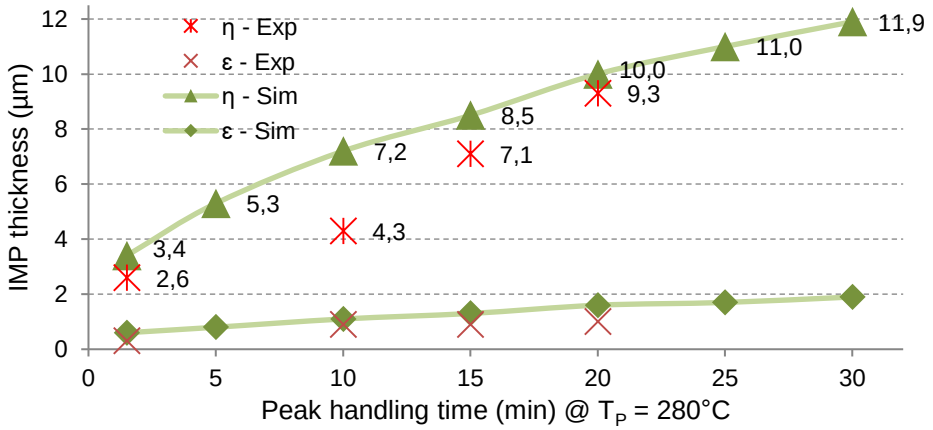


Figure 63: IMC growth comparison of experimental and simulated Cu_6Sn_5 and Cu_3Sn phases over handling time (t_h) where, T_p= 280 °C, $\Delta_H = \Delta_C$= 2.5K/s.

It can be inferred that the initial copper available in the solder paste and copper from substrate interface forms Cu_6Sn_5 quickly during the first few minutes corresponding to the critical interlayer thickness in thin-layer

TLPS joints, which can be explained for comparatively lower η-IMP formation until 10 min. However upon prolonged thermal treatment, the liquid tin during expansion phase as explained in sub-chapter 3.1, comes in contact with copper from the ε-phase and substrate for further η-phase formation. The ε-phase thickness was found to be constant between 1 to 1.6 µm even with increased handling time up to 30 min. The results of obtained IMP values of peak temperatures (T_P = 280 °C) are shown in Figure 61. In this case, the tests were performed only up to t_P of 20 minutes. Compared to the peak temperatures of 260 °C, the η-phase had similar values with increasing peak time. However, in case of 280 °C, the η-phase reached upto 10 µm in 20 min compared to 25 min peak time of 260 °C. The ε-phase growth was also constant in this case similar to above 260 °C profiles. Figure 63 shows the IMP growth in samples at peak time of 10 min and 15 min respectively. With increase of time, though the height of the grains was similar, the scallopial structures obtained diameter increase which indicated the IMP formation between the individual grains. This grain growth can also be observed in Figure 60.c,d. Table 20 shows the experimental and simulated result of IMC thicknesses for tested profiles of Model 3. The results obtained show that the modelled and experimental values are near in case of η-phase, however not in case of ε-phase.

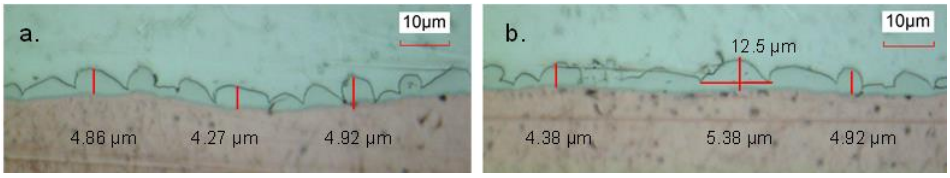


Figure 64: Influence of peak time on SC substrate on η-Cu_6Sn_5 formation for T_P = 280 °C, t_P: a.= 10 min; b. = 15 min.

Table 20: Comparison of simulated and experimental average IMP thickness for tested profiles with post-handing time

Peak holding time at 260 °C [min]	Annealing/ Post-handling time at 210 °C [min]	Sim η (Cu_6Sn_5) IMP [µm]	Sim ε (Cu_3Sn) IMP [µm]	Exp. η (Cu_6Sn_5) IMP [µm]	Exp. ε (Cu_3Sn) IMP [µm]
10	10	6.3	1.0	6.48	0.93
10	5	6.1	1.0	6.31	1
5	10	5.2	0.8	3.68	0.5

6.2.2 Outlook for Optimization of TLPS Process

Based on the simulation and preliminary investigations to check the time needed for full η- transformed bondline, two basic profiles were initially tested with VVP soldering with prolonged peak time at 260 °C to check the phase formation on SC substrates ($R_z \leq 16$ µm) for a 20 µm solder paste height. The main difference in this case is the use of the silicon components i.e. 2.3 mm x 2.3 mm x 500 µm resistors and soldered in a VVP soldering machine with vacuum of 15 mbar with profiles shown in Figure 65. The profiles had a peak time of 6 min and 15.5 min respectively. The vacuum activation in the VVP machine was possible only at the end of the peak time. To lower the void percentage and to obtain accurate copper-tin IMPs in case of thin solder layers, the flux material were dried out after paste printing and component placement in a heating oven at 120 °C for 5 min. The obtained IMP values for these VVP profiles are shown in Figures 66, 67, 68 and 69. The former two figures show the IGBT cross-sections and latter two figures show the cross-sections of the resistors chips. Firstly, it can be observed that the η-IMP formation depends mainly on the substrate roughness, which indirectly reduces the gap between the components. It can also be observed from the figures also that the IMP formation as explained in the sub-chapter 3.1 is directly influenced by the process time.

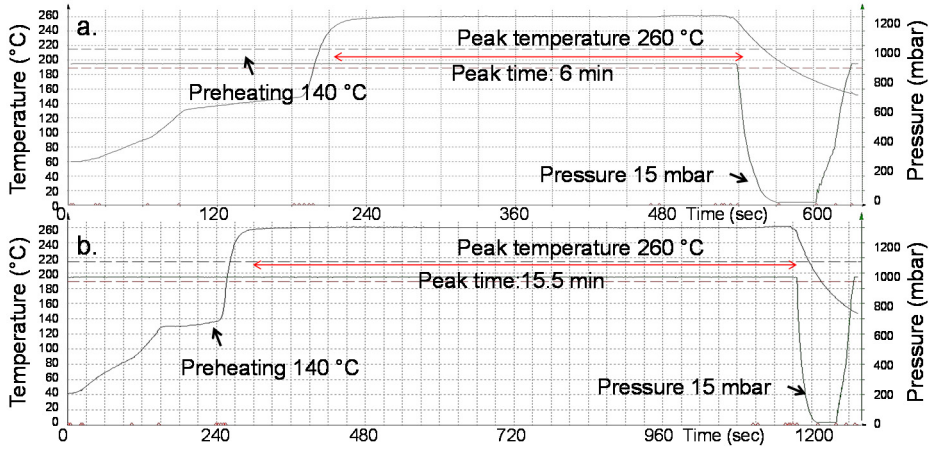


Figure 65: Recorded test profiles for VVP soldering with peak temperature of 260 °C for peak and total profile time of a. 6 min, 10.5 min; b. 15.5 min, 22 min.

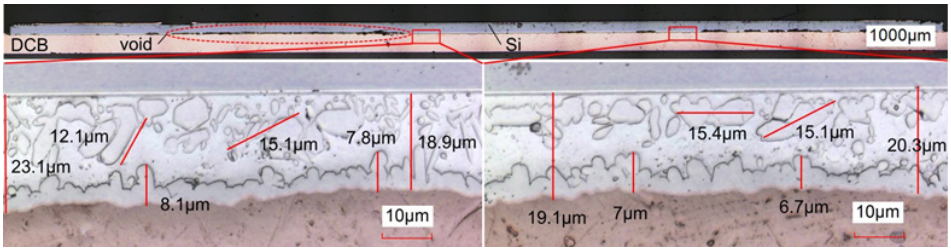


Figure 66: Cross-section of the soldered IGBT for profile with peak time of 6 min.

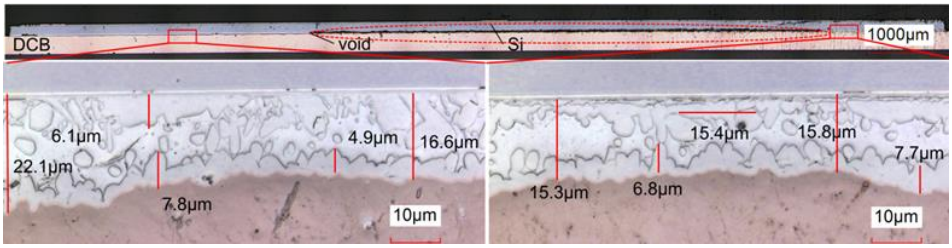


Figure 67: Cross-section of the soldered IGBT for profile with peak time of 15.5 min.

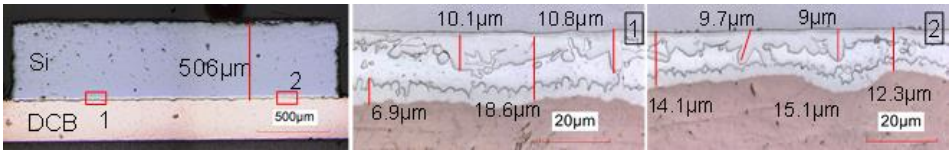


Figure 68: Cross-section of the soldered resistor for profile with peak time of 6 min.

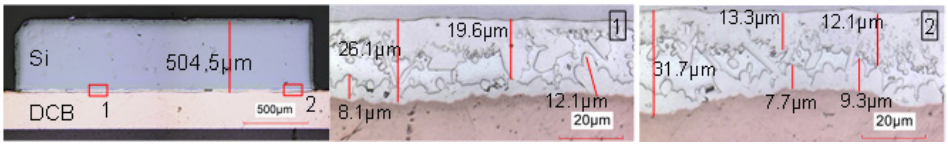


Figure 69: Cross-section of the soldered resistor for profile with peak time of 15.5 min.

In comparison to Figure 60 for the η-IMP, the thickness at the substrate side agrees with the simulation and the preliminary analysis due to abundance of copper from the substrate as observed in all figures and cross-section of the soldered IGBT for profile with peak time of 6 min at approximately 7 µm for 15 min peak time. A similar IMP thickness was also observed for 5 min peak time. The growth as observed in form of scallops of average height of 3 - 4 µm and highest peaks of 6.5 µm for peak time of ca. 6 min. The agglomerated scallopial structures had an average height between 6 - 8 µm for longer peak time. However, on the chip side, the IMP formation was comparatively slower and in form of clustered islands in the bondline in Figure 65. These were formed due to the available copper in the solder material. The agglomeration of these islands can also be observed

with extended peak time as seen in Figure 66. But the IMP phase formation was also dependent on the component size along with the influential factors like peak temperature and time, i.e. energy transfer efficiency to the solder material. Compared to the large components, the smaller components had homogenous energy input which let to increased IMP formation that can be observed in both interfaces at component and substrate sides as in Figure 68 and 69. However the voids for the assemblies were relatively at more than 25 % and 35 % for 6 min and 15 min peak time respectively. This was observed irrespective of the component size for the 20 µm solder printed joint with resultant average bondline thickness of 15 µm. A direct influential factor in the IMP formation is the void formed during the flux burn-out and tin usage during the soldering process. An overview of the voids formed during the diffusion soldering and the measures taken to improve the quality are explained and summarized in the following chapters.

6.3 Void Analysis for Thin-film Solder Interconnections

Generally in case of normal solder interconnections in electronics production, the voids in the bondline increase with decreasing solder thickness. However, a special vacuum process step during soldering is demanded for absolutely void free solder joints [185]. Though vacuum process is associated with some essential disadvantages, it produces absolutely void-free joints with high yield for solder heights above 200 µm. The type of voids that occur during the outgassing of the residual gasses and cooling leads to shrinkage voids sometimes observed with improper profiling and pressure release. Besides the technical expenses for vacuum pumps and additional locks, the vacuum process excludes the use of gas convection for heating and cooling. Apart from a special vacuum vapor phase technology, most machines are using infrared radiation or heat conduction for soldering. The same principles as used in vacuum soldering technology are applicable also for a higher pressure level. If the void in the solder joint is arising for an excess pressure, the normal atmosphere pressure could be sufficient for escaping of enclosed gas [170]. Essential for this effect is the pressure difference between inside and outside of solder joint. A benefit of soldering with excess pressure is the possibility of gas convection for heat transfer. This allows the application of conventional components and the realization of the usual temperature distribution and profiles. In this work are the above explained void-reduction mechanisms of vacuum and overpressure techniques are focused for interconnects with thicknesses from 110 µm down to 20 µm. This is attributed to the difficult outgassing of the gasses

during flux burnout. For void-free interconnec-tions, a void reduction technique is inevitable. According to the state-of-the-art machine concepts, vacuum soldering is well known technique to obtain interconnects with voids percentages less than 5 % for solder layer thicknesses down to 80 µm. But it is however limited to conventional SMD assemblies. In case of power electronics, the component sizes vary from 1 mm² to more than 100 mm², and as explained in above sub-chapter on the requirements for thin void-free bondlines, an efficient and reproducible solder profile is absolutely necessary. A few investigations were performed to observe the influence of the solder height with a conventional reflow machine 'ERSA Hotflow 2/14' with die size of 100 mm² and Type 6 F640 SAC305 solder paste. It can be observed clearly from the Figure 70 that with the decreasing bondline thickness of approximately 150 µm, 100 µm and 60 µm printed solder pastes, the obtained voids increased exponentially to 8, 21 and 63 % respectively. In this context, the preliminary profile optimization for obtained low-void interconnects was performed for the vacuum vapor phase soldering technology and then further customized for the overpressure convection machines.

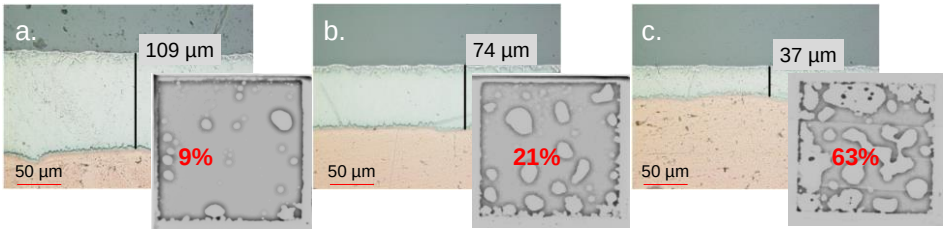


Figure 70: Increase of void percentages for SAC305 type 6 solder paste with decrease in solder paste thickness a. 120µm, b. 80µm and c. 60µm.

As introduced in section 4.2, the soldering machine used in the module construction was a vacuum equipped vapor phase soldering machine IBL VAC645 (VVP) capable of vacuum down to 20 mbar during peak time with 260 °C galden medium. The usage of this high-temperature medium was necessary due to the used $Sn_{99.3}Cu_{0.7}$ solder pastes with melting range between 227 to 240 °C and to ensure minimum of 255 °C temperature on the copper substrates due to high thermal mass. The profile used was as introduced in sub-section 4.1.2, but with multi- or stepped vacuum control as shown in Figure 71.

During the commissioning, numerous profiling attempts were done in the beginning to obtain the suggested stable process conditions for the new solder pastes and galden medium; the main difficulties were the temperature control on the substrate and the substrate carrier followed by the

temperature gradient and vacuum control due to intensive energy transfer of the vapor medium. The profiles were tested with the software updates of vacuum control mainly single vacuum, double vacuum and stepped vacuum.

The test samples in this case were the 10x10 mm² bare-dies with solder paste thickness of approximately 40 µm on SPC substrates of roughness $R_z \leq 16$ µm. The double vacuum showed good result with lower voids of ~4% compared to other variants as shown in the Figure 72. A further reduction was possible with the increase of the gas absorption power of the vacuum pump, but due to low solder heights, components less than 25 mm² were unstable and flipped into the liquid medium. It was inferred that void rates down less than to 3% and 1% were possible for smaller components between 1 - 6.5 mm² contact area and thicker solder paste thicknesses greater than 80 µm due to easier outgassing. After the evaluation of the assemblies from VVP machine, it was concluded that multiple pressure cycle variation significantly reduces the void percentages.

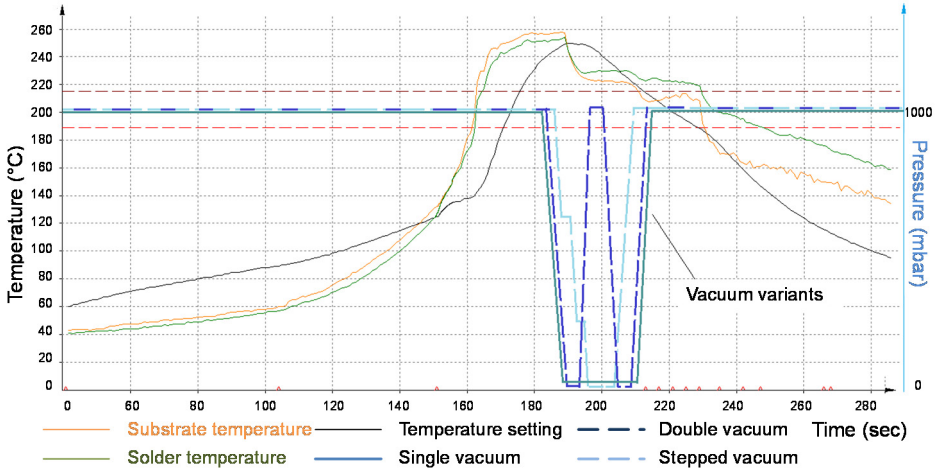


Figure 71: Vacuum vapor-phase solder profile variants with 20 mbar at 260 °C.

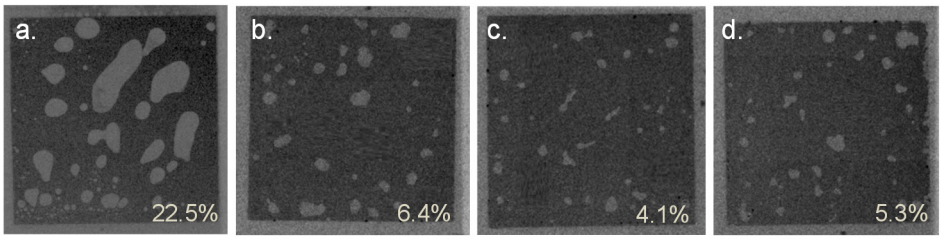


Figure 72: X-ray images of semiconductor dies of size 100 mm² for solder profiles with a. no vacuum; b. single; c. double; d. stepped variants

Further the reflow convection soldering machine 'Seho MaxiReflow HP' (OPC) capable of building pressure up to 5 bar (absolute) in peak temperature chambers was tested for the first time for assemblies with solder heights of 20, 60 and 110 µm on SPC substrates with roughness $R_z \leq 5$ µm. The profiling of the OPC machine was comparatively complex due to numerous influential parameters. The main aim was to find optimal pressure and temperature settings to obtain an interconnect with low voids for solder thicknesses down to 20 µm. Table 21 shows the settings for temperature profiles for Squeeze-release-squeeze-freeze (SRSF) overpressure variation at peak temperature in the hyper pneumatic chamber. A short overview of the SRSF point the chamber positions cp1 and cp2 is given in Figure 72. The blue curve (in air) shows the sudden changes in temperature during pressure changes recorded by the thermo-element used to measure the surrounding temperature. It should be observed from the figure that for the SRSF cycle, the first and second pressure build-up up to e.g. 3 bar are at peak temperatures at cp1 position, only after the substrate moves into chamber position cp2 i.e. less than 227 °C below liquidus temperature, is the pressure released to hold the reduced void content in the interconnection.

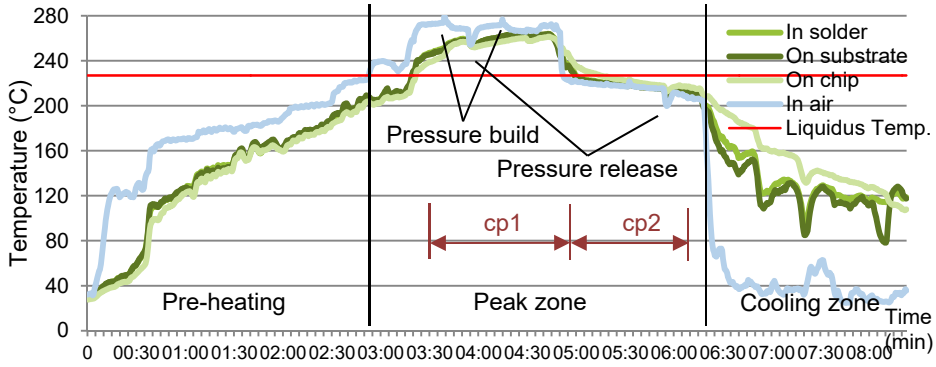


Figure 73: Recorded profile from the OPC machine showing the 1xSRSF in the chamber positions cp1 at 295 °C and cp2 below liquidus temperature 227 °C.

The settings for the tested profiles from Table 21 show that the settings must be accurately varied for a change in pressures cycles accordingly. It much be absolutely checked with the time settings mainly at the chamber positions that a significant void reduction is obtained. Table 22 shows the test profiles 1 to 10 for various settings in pressure chamber with main focus on the SRSF cycles and the time settings between the pressure variations. The basic profile setting was done for profile 1 for the solder material $Sn_{99.3}Cu_{0.7}$ with liquidus temperature at 227 °C. The installed cp1 temperature i.e. TP was 285 °C and cp2 at 185 °C.

Table 21: Settings of the temperature profile with SRSF for the OPC soldering

	Pre-heating (90 cm/min)						Peak zone		Cooling	
T_{top}	170	180	190	200	205	-	cp1	cp2	28	26
T_{bottom}	170	180	190	200	205	250	285	185	28	26
1xSRSF Profile 1;	Hold time before SR (15s), **s**queeze (3 bar, 15s), **r**elease (1 bar, 5s before SF), **s**queeze (3 bar, 55s), into cp2 **f**reeze (10s, 1 bar)									
2xSRSF Profile 3;	Hold time before SR (15s), **s**queeze (3 bar, 15s), **r**elease (1 bar, 5s before SR), **s**queeze (3 bar, 15s), **r**elease (1 bar, 5s before SF), **s**queeze (3 bar, 55s), into cp2 **f**reeze (10s, 1 bar)									

Table 22: Overview of the tested profile variants in the overpressure convection soldering system with preheating temperature gradient of 2.5 K/s

Profile Nr.	T_p [°C]	Pressure abs. [bar]	SRSF Cycles	Further changes in the profiles
1	285	3	1x	Release (1 bar, 5s) between pressure cycles
2	285	3	1x	Release (1 bar, 15s) between pressure cycles
3	285	3	2x	Double SRSF, normal wait time
4	285	5	2x	Double SRSF, increased pressure at 5 bar
5	295	3	1x	Increased preheating temp. 205 -> 230 °C, peak temp. 285 -> 295 °C T_P
6	295	5	1x	
7	310	5	1x	Increased T_P for stabilization, higher pre-heating 205 -> 230 °C, slower preheating 75 cm/min, hold time before SR (30 s)
8	310	5	2x	
9	285	3	1x	Profile 1; faster transfer into cp2 (5s)
10	305	5	1x	Faster preheating time 120 cm/min, faster transfer into cp2 (5s)

The temperature was eventually increased to adapt to the power electronic substrate i.e. increased thermal mass compared to conventional PCBs and the pumped process gas into the pneumatic chamber for pressure buildup. As the pumped gas was at ca. 20 °C i.e. less than surrounding temperatures,

it can be observed from the Figure 73 that the settings needed to be changed to keep the temperature in the enclosed chamber stable above the liquidus temperature. With increased pressure value or with multiple pressure cycles, a difference of at least 10-15 °C of the chamber temperature was observed. The stabilization of the reduced heat was possible by adaptive heating from the additional radiators inside the pressure chamber. The temperature profiles 5 and 6 are to observe the void variation accordingly for above arguments. The profile 7 and 8 also are adapted profiles with additional heating of the assemblies to ensure proper outgassing of the flux components before pressure variations. The profile 9 and 10 were designed to observe the effects of shortened profile time increased transport band speed and with reduced peak time respectively. The profiles 1 to 6, 7 to 9 and 10 had the transport band speeds of 90, 75 and 120 cm/min respectively.

The Figure 74 shows the obtained average void percentages of the NiAg metallized (i.e. DN1, DN2, DN3) and copper metallized dummy components (i.e. DC1, DC2, DC3) respectively. The numbering corresponds to the increasing contact surface area of the components i.e. 6.25, 25 and 100 mm². Here for the tests '5, 3 and 1' number of components were taken for each tested profile respectively for each component size. A decreasing void trend can be seen in the profiles from P1 to P8 for solder thickness 110 µm, where the void percentages were less than 3% for smaller components and less than 8% for larger components of NiAg metallizations. This shows an increasing void content with increasing solder contact area. However the trend flattens with reducing solder thickness. It was extremely difficult to attain void percentage less than 5 % for all component dimensions 25 mm² or higher. The trend lines for the smaller components show that the average void percentages rise with decreasing solder heights. For 20 µm solder layer thickness, the void percentages were at 10% for most of the profiles.

For the copper metallized components, the void content was relatively high due to oxidation of the component metallization. The void content was more than 35 % to 60 % according to the solder height. It must be noted that all the tests were performed under normal air instead of nitrogen to reduce the machine costs during experimentation. A 2X SRSF profile with ΔP = 4 bar consumes almost 1000 litres of nitrogen. The profiles 7 and 8 were selected as optimized profiles with 1x and 2x SRSF for the further testing for TLPS for the power electronics substrates irrespective of the component type due to obtained low void percentages.

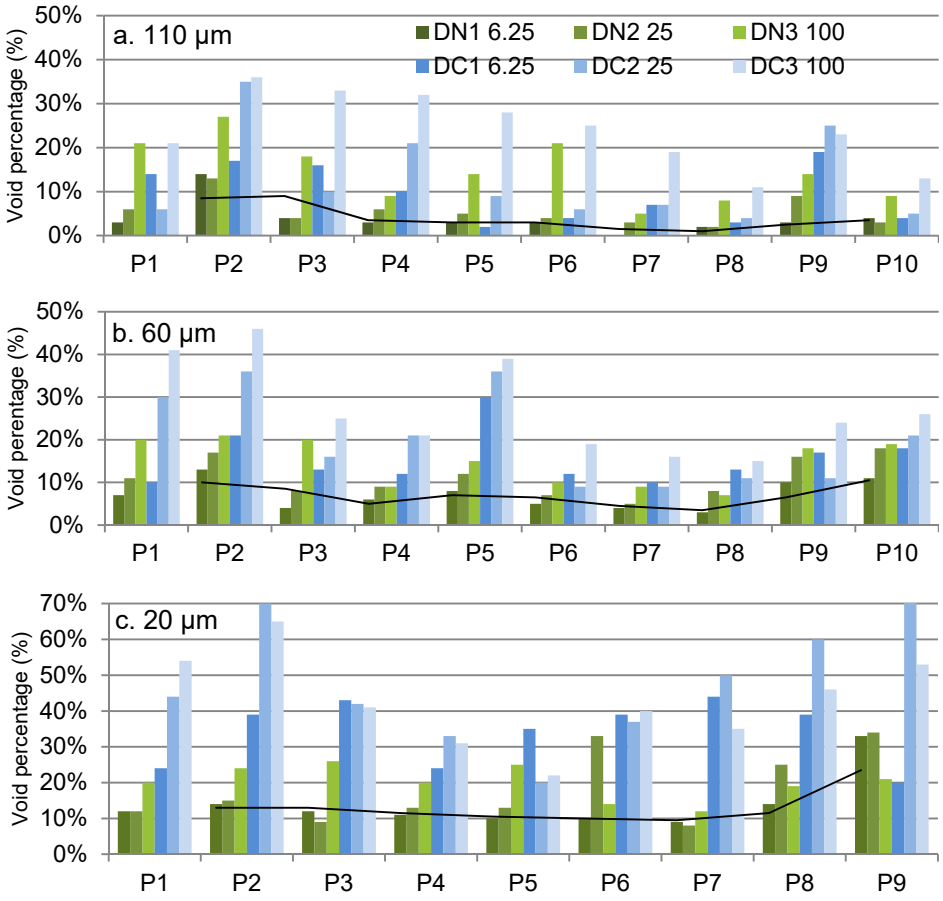


Figure 74: Overview of the void percentages with solder paste thickness and the over-pressure profiles P1 to P2 from Table 22 for 110, 60 and 20 µm solder layers

6.3.1 Investigations for the Preform based Interconnections

As summarized in Table 16, the preforms B1P1 and B1P2 were tested for wetting under formic acid and forming gas environment in the CFL machine introduced in sub-chapter 4.2, on bare copper (SPC) and nickel plated (SNC) DCB substrates. The preforms and components were placed on the DCB substrates were treated with formic acid in preheating zone and soldered under formier gas at 260 °C. According to the preform material supplier, the melting points of the non-eutectic compositions were between 235 °C and 250 °C. To check the wetting characteristics, the soldering of ~25 µm thickness preforms was performed for 26 mm² dies with 18.5 mm² preforms. As shown in Figure 75, it can be observed that formic acid had no influence on Ni-DCBs showing poor wetting. In case of Cu-DCBs, the liquid

tin spread throughout the entire chip area. The preform B1P1 showed good void percentages on Cu-DCB (<0.2%) in comparison with Ni-DCB (~2%). The Ni-DCBs were passive to the formic acid handling. The presence of Ni content in B1P2 also evidently increased the voiding due to poor wetting characteristics. It was observed that due to poor wetting, the resultant bondline has increased thickness. In case of B1P2, the void contents were ~3.2% on Cu-DCBs and ~5% on Ni-DCBs. The wetting of the preform on the component surface directly influences the final TLPS bondline thickness, which is explained in further sub-chapters.

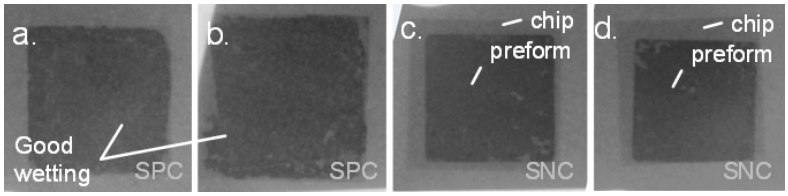


Figure 75: X-ray images of CFL soldered 5.1 mm x 5.1 mm Si-chips with preform B1P1 (a) and B1P2 (b) on SPC Cu-DCB and B1P1 (c) and B2P2 (d) on SNC Ni-DCB with 2.5 min peak time.

Table 23: Overview of the used substrate materials and resultant bondline thickness measured through cross-sectional analysis.

Chip size	5.1 mm x 5.1 mm			
Solder preform size	4.3 mm x 4.3 mm			
Preform thickness (µm)	22.5 ± 2.5			
Bondline thickness on substrates (µm)	Substrate	Preform	B1P1	B1P2
	Cu - DCB (SPC)		**14**	**16**
	Ni - DCB (SNC)		**28**	**26**

Table 23 shows the obtained bondline thickness for the assemblies using the preforms. Due to improper wetting on the nickel DCBs, the bondline was slightly increased. In case of copper substrates, the wetting was uniform and bondline were reduced down to average of 15 µm as expected. Further Figure 76 shows the X-ray images of preliminary assemblies prepared by using the new thin preforms with components of same size i.e. 18.5 mm² dies with 18.5 mm² preforms. This indicated the similar poor wetting characteristics for Ni-DCBs. However, excellent void percentages less than 2% were observed for Sn-Cu preforms on Cu-DCB substrates compared to >5% for Sn-Cu-Ni preforms on Ni-DCB substrates. The wetting of the preforms on copper surfaces with low roughness was comparatively good to solder pastes.

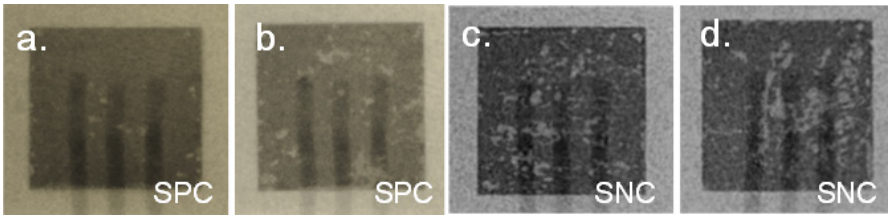


Figure 76: X-ray images of 400 µm wire-bonded 4.3 mm x 4.3 mm Si-chips CFL soldered with preform B1P1 (a) and B1P2 (b) on SPC Cu-DCB and B1P1 (c) and B2P2 (d) on SNC Ni-DCB with 2.5 min peak time.

6.3.2 In-situ X-ray Investigation for TLPS Profile Optimization

As introduced in sub chapter 4.1, the main idea of the developed in-situ test setup by Mr. Klemm [173] was to check the feasibility for an automated analysis of the soldering process to analyze the test assemblies for voiding and materials related influences. The main aim was also to optimize the solder profile with void reduction and modification of influential process parameters. Mr. Klemm as part of his research work in two public funded projects 'HotPowCon' and 'ProPower' developed the in-situ system for analysis of solder materials with varying flux materials for power electronic applications

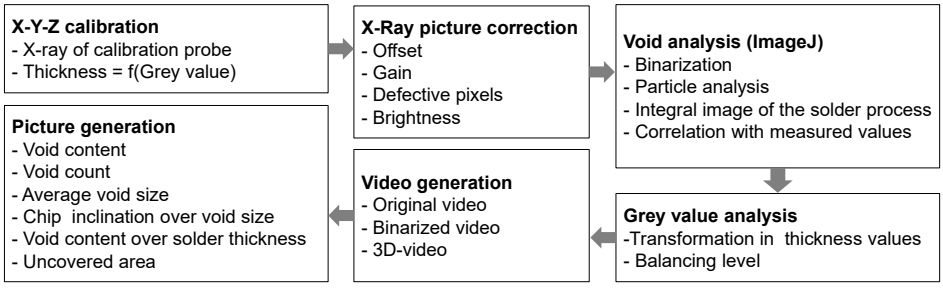


Figure 77: In-situ analysis workflow followed for TLPS profiles in this work.

As part of the research work on hand, the assemblies were tested for the modification of the developed TLPS temperature profiles for further modification and optimization by using the In-situ measurement set-up. As shown in Figure 77, the analysis workflow followed was similar to Klemm, where the preparation of assemblies was performed at Institute FAPS, Nuremberg and the in-situ soldering and recording was performed at Institute for Electronic Packaging Technology (IAVT), Dresden.

The post-recording analysis was performed at Institute FAPS. For the picture analysis, the software ImageJ was used extensively for image analysis. The scripts and corresponding macro functions from Klemm [173] were used by slight modifications with respect to analysis window, threshold settings and output generation. The set-up and the post-analysis algorithms were further developed by Mr. Klemm to investigate using integral overlap where the areas for improper wetting and outgassing characteristics with respect to the solder thickness and profile parameters are investigated. The output files from the post-analysis from this work contained mainly the void content, void area, average void size and uncovered area of the chip.

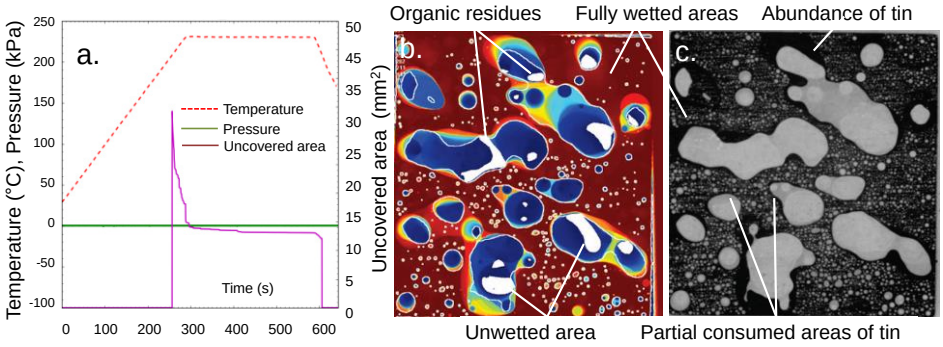


Figure 78: a. In-situ temperature profile showing the uncovered area under the chip; b. Integral image over time; c. In-situ X-ray image for peak time of 5 min.

Figure 78.a shows an example of a solder profile with 230 °C peak with no pressure change measured in the in-situ chamber. And Figure 78.b shows the integral image of a soldering profile over time by Mr. Klemm [173]. The white-filled areas represent areas which were detected as never wetted or soldered during the entire soldering process. The white borders show the outlines of the pores present in the final state in the solder joint. The red colored areas in the integral images show the sum of all times in seconds, in which the relevant pixel was detected as covered with solder. In almost all soldered soldering spots, individual surfaces could be identified which were detected as never soldered during the entire soldering process. The temporal development of the integral image is also fixed by storing each intermediate result and summarizing it later in a film. Thus the development of the integral image over time can be understood with little effort. After each recalculation of the integral image, the area of all the pixels which have never been covered with solder was also measured. This results in the diagram shown in Figure 78.a. Since the data acquisition is based on the period between melting and solidification of solder, the covered area outside this period were set to the value zero.

The following points were investigated with the in-situ X-ray set-up in case of diffusion soldering:

- How does the interlayer material react to the pressure changes (i.e. vacuum/ overpressure) during the peak temperatures?
- Is the outgassing behavior at overpressure different from that at vacuum?
- How does the timing of the pressure change influence the resultant void content?
- How is void content influenced by changes in time and temperature?
- Is the absolute pressure difference or the relative pressure ratio decisive for the effect of void reduction?
- Can the diffusion controlled isothermal solidification be observed or tracked with temperature and time?
- Which types of defects are observed in case for prolonged heat treatment?
- What are the effects of the substrate or interlayer properties on the void formation?

To understand the two void reduction mechanisms, in-situ X-ray analysis was performed initially for conventional temperature profile with modified pressures, where the variations in void content could be actively observed, recorded and investigated. Numerous samples were soldered with in-situ X-ray device with the changes in pressure, peak temperature and peak time.

The standard profiles introduced in the subchapter 4.2 were also simulated with a 10mm x 10mm semiconductor chip on DCB substrates to analyze the void variation. Due to in-situ device limitations, the pressure could be varied down to 0.2 bar and up to maximum 3.2 bar (i.e. ΔP = 2.2 bar) and peak temperature up to 250 °C. Figure 79 and 80 shows the recorded images for analysis of the temperature profiles with vacuum and overpressure respectively. It must be noted that the energy transfer mechanism was heat conduction from the baseplate under the substrate. Figure 79 shows 10 process points for the vacuum profile settings as in Table 24. The figure shows that the flux is activated from 150 °C and the solder starts melting at 225 °C (Figure 79.d) followed by natural outgassing of gas bubbles (Figure 79.e) till vacuum activation. Here the vacuum was activated after no significant outgassing was observed as in Figure 79.f. Even at such negative pressures, the outgassing continued as in Figure 79.g,h.

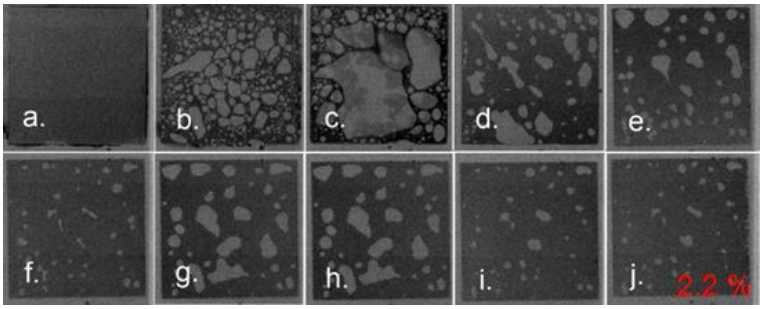


Figure 79: In-situ X-ray recording with variation in voids as in Table 243 for a standard vacuum solder profile of 200 mbar.

Table 243: Process parameters for the recorded vacuum profile of Figure 7 (a-j)

Figure 79	t_{rec} (sec)	T (°C)	P (bar)	ΔP (bar)	Void percentage (%)
a	0	35	1	0	0
b	170	160	1	0	30.9
c	220	225	1	0	53.3
d	230	230	1	0	18.98
e	240	240	1	0	13.2
f	242	240	0.2	-0.8	2.6
g	250	240	0.2	0	13.8
h	255	240	0.2	0	13.9
i	260	210	1	0.8	2.3
j	275	190	1	0	2.2

The ventilation of the chamber and cooling of assembly must happen simultaneously to assure a reduced void percentage i.e. 2.2%. The maximum void percentage up to 55% was observed during the flux outgassing i.e. pre-flow phase of the solder profile. Figure 80 shows the over-pressure soldering process explained with 10 points with process parameter change. A similar flux activation and solder melting (Figure 80.c and Figure 80.e) was observed as in Figure 80.b-d. SRSF process can be clearly seen in series of pictures (Figure 80.e-i), where the voids are reduced to 2.9% upon 3.2 bar pressure build-up (Figure 80.f).

There must be enough time available before over-pressure activation for natural outgassing. An early pressure build-up hinders the natural outgassing, which may affect void percentage at later point. New voids are not formed as the over-pressure hinders the void formation (Figure 80.f, g). The second squeeze effectively reduces the voids further compared to first squeeze. The void percentage stays constant as the assembly is cooled below melting point before pressure release (Figure 80.i, j).

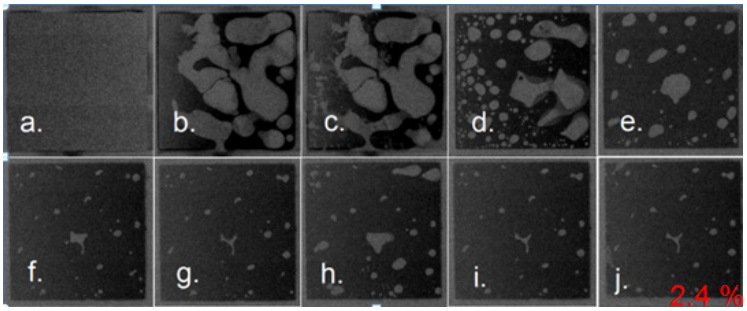


Figure 80: In-situ X-ray recording with variation in voids for an overpressure solder profile of relative pressure 2.2 bar.

Table 25: Process parameters for the recorded overpressure profile of Figure 80.

Figure 80	t_{rec} (sec)	T (°C)	P (bar)	ΔP (bar)	Void percentage (%)
a	0	32	1	0	0
b	80	145	1	0	42.1
c	135	180	1	0	43.1
d	190	220	1	0	28.4
e	195	240	1	0	11.2
f	230	240	3.2	2.2	2,9
g	240	240	3.2	0	2,9
h	243	240	1	-2.2	7.4
i	250	240	3.2	2.2	2.4
j	275	180	1	-2.2	2.4

After the above preliminary analysis to understand the effects of the pressure variation, various tests were performed with combined vacuum and overpressure. It was summarized that a combination of vacuum and overpressure at critical points immensely reduces the void percentages. The results of the in-situ investigations are summarized in the dissertation 'In-situ characterization of soldering process for power electronics ' by Mr. Klemm [173]. The combined profile suggested also by Mr. Klemm was further used to modify the thermal treatment profiles and test practically for diffusion soldering in this work. However, the actual positions where the vacuum and overpressure are to be activated and maintained were still to be investigated in actual soldering machines. This part is covered is the present dissertation with respect to the combination of pressure changes along with process gasses for high-quality diffusion soldering.

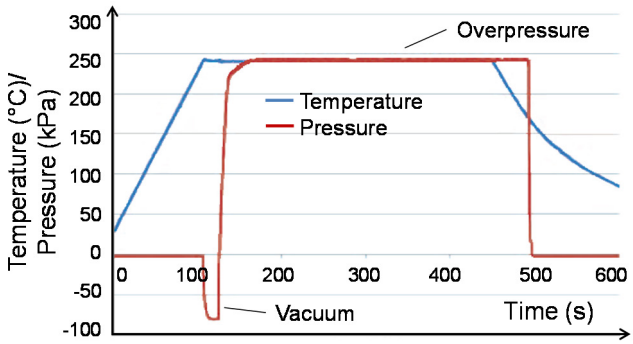


Figure 81: Combined soldering profile with vacuum and overpressure settings used for the in-situ investigations.

The following results from the previous investigations were considered for the investigations in diffusion soldering:

- For each soldering process the void content reaches a minimum shortly after the melting of the solder.
- Overpressure slows down the growth of voids.
- Negative pressure speeds the growth of voids up and helps to use up the reactants in the solder paste more quickly.
- Negative pressure allows a higher void reduction with less technical complexity than overpressure.

The in-situ investigations revealed that higher heating rates showed a faster decrease of solder uncovered area after flux evaporation. A slower heating rate resulted in larger unwetted areas and consequently increased the final void percentages.

For the further tests, based on the analysis, a new optimized profile was designed combining the vacuum and overpressure. Here the vacuum was activated at the beginning of the profile after complete natural outgassing and for IMP formation, an extended peak time with over pressure was considered. Figure 81 shows the recommended diffusion soldering profile based on the comprehensive in-situ X-ray analysis. The contrast-to-noise ratio (CNR) of the images was too low for a reliable automated analysis of the X-Ray videos. However, some differences between conventional soldering and the diffusion soldering process could be identified, discussed in latter part of this section. The profile was designed with the following specifications. The heating rate of 2 K/s was considered for the pre-heating step. The duration of vacuum step of around 10 seconds was considered after the solder has molten. A rapid change to overpressure for decelerated outgassing. The IMC formation is accelerated by simulated overpressure

environment at peak temperature. The overpressure is released after the temperature is down to less than the solidus temperature of the solder.

The prepared test assemblies with bare Cu-DCB with Sn-Cu solder and silicon chip were analyzed in the in-situ X-ray device. The heating gradient was limited to a maximum of 2 K/s. A peak temperature of 260 °C was selected for in-situ diffusion soldering investigations. For the tests, solder paste $SnCu_{0.7}$ type 6 was used and stencils with thickness of 20 µm and 60 µm were used for solder paste printing on bare Cu-DCB substrates. The substrate variants with roughness of SPC $R_z \leq 5$ µm and SC $R_z \leq 16$ µm were used to observe the outgassing characteristics and IMC growth in dependence to substrate roughness. Profile time of 15 min was taken with peak time of approximately 11 min.

Influence of the pressure change

In Figure 82, Figure 83 and Figure 84 along with the temperature and pressure settings, the void content (left) and also the uncovered area with time (right) for solder thickness of 20 µm and 60 µm with variation in substrate roughness are represented. The pressure change with combined vacuum and overpressure had considerable change in the resultant void content in comparison to the only vacuum or only overpressure profiles. It can be observed clearly that the vacuum activation upon solder melting helped in the rapid decrease of the void content and the solder wetting under the chip. The assemblies were most influenced by the activation of vacuum and rapid building of the overpressure, which suppressed and significantly decelerated the gas production. This allowed maintaining the void percentage constant for prolonged profile time.

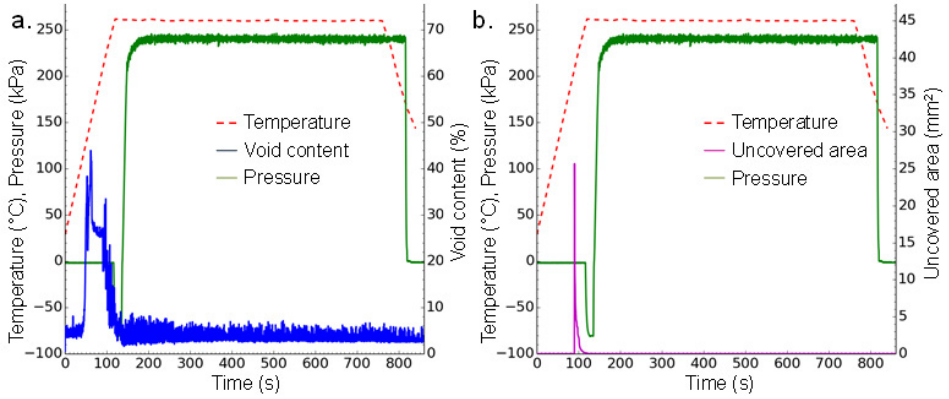


Figure 82: Void content and the uncovered area of substrate SPC ($R_z \leq 5$ µm) with 20 µm solder paste thickness.

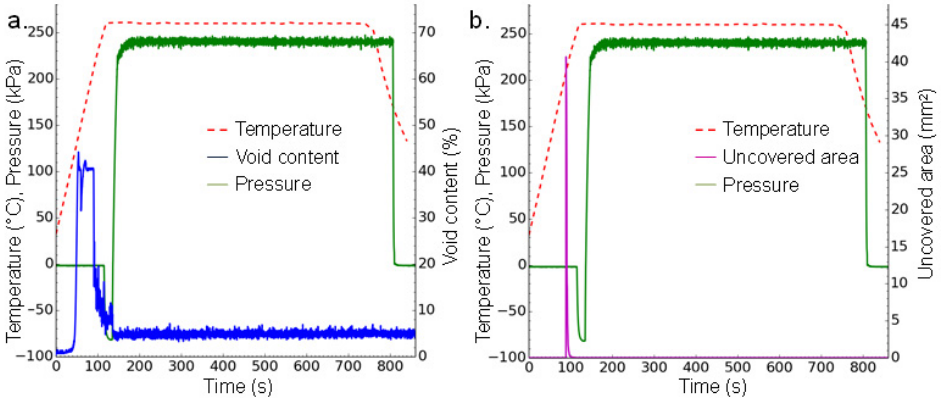


Figure 83: Void content and the uncovered area of substrate SC ($R_z \leq 16$ µm) with 20 µm solder paste thickness.

Influence of the substrate roughness

It was observed that the roughness of the substrate played also a major role in the initial outgassing characteristics of the flux agents. The rougher topography resulted in higher void content compared to smoother substrates. This could be due to easy outgassing during the pre-heating phase and at the molten state. For the solder thickness of 20 µm on a substrate with $R_z \leq 16$ µm, the outgassing as observed was relatively difficult also during the initial phases, which eventually could have been due to the trapped gas. It was observed on numerous samples that the roughness of the substrate had less influence in the final void percentage at the end of the profile.

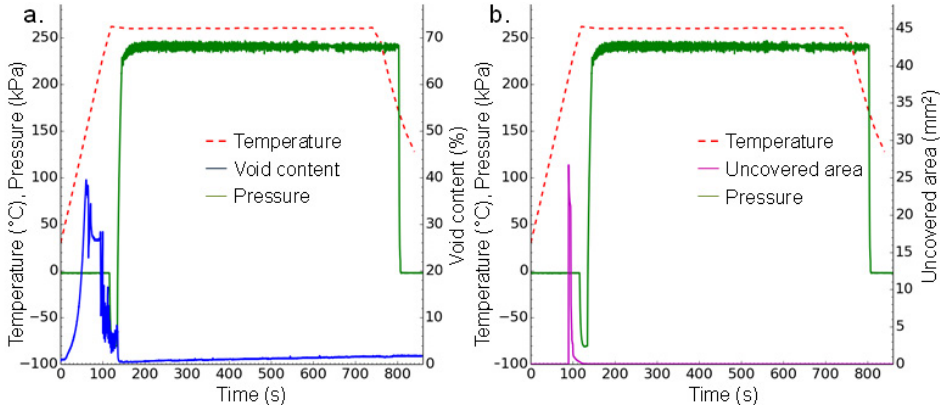


Figure 84: Void content and the uncovered area of SPC ($R_z \leq 5$ µm) with 60 µm solder paste thickness.

This can be observed in the uncovered area representation in Figure 82 and Figure 83, where the uncovered area was approx. 25 mm² and 40 mm² for substrate roughness of 5 µm and 16 µm respectively. Figure 85 and Figure 86 show the in-situ images of the samples with solder thickness of 20 µm and varying roughness for profile measurements as in Table 26. It can be observed that at initial phases of heating in case of sample with roughness 16 µm, the escape of the gas occurred in form of small canals. This was however not observed in case of solder thickness of 60 µm. The observations indicate that the rough surfaces produced micro-voids upon prolonged handling time. This can be observed also in Figure 80 and Figure 86. It must also be noted that compared to the thicker solder deposits, the maximum void percentages of up to 80% were observed in thin solder layers during preheating phase.

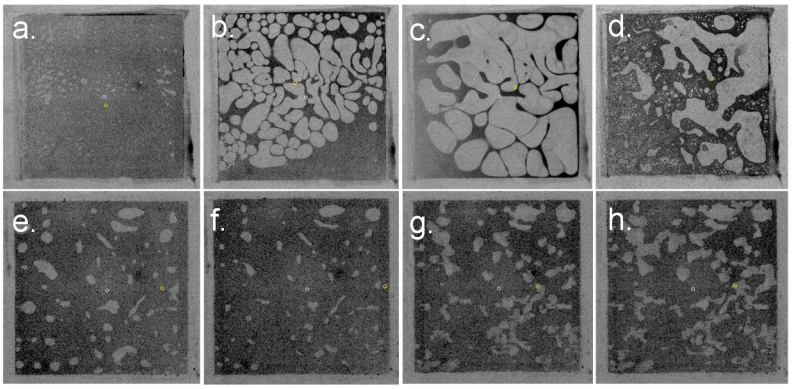


Figure 85: In-situ X-ray recording with variation in voids for a TLPS profile for substrate SPC with $R_z \leq 5$ µm and solder height of 20 µm.

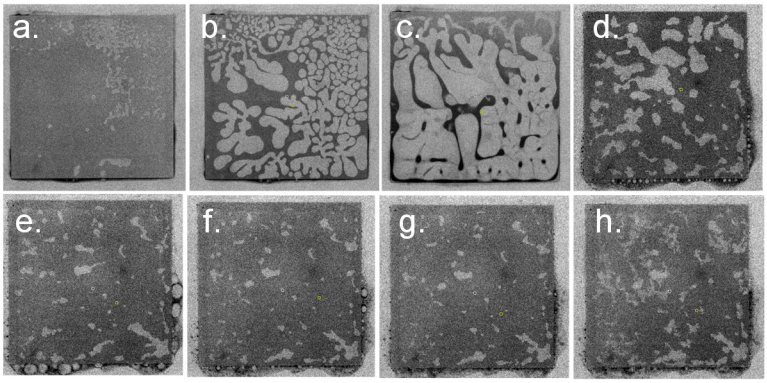


Figure 86: In-situ X-ray recording with variation in voids for a TLPS profile for substrate SC with $R_z \leq 16$ µm and solder height of 20 µm.

Table 26: Process parameters and void percentages for the investigations for Figure 85 and 86 with vacuum and overpressure combination.

Position	Phase of solder profile	Fig. 85, void %	Fig. 86, void %
a	After chip placement	-	-
b	$T_{process}$ @ 145°C	40.8	44.5
c	Solvent burnout	56.1	68.2
d	Solder melt phase	32.6	20.6
e	Vacuum activation -80 kPa	12.9	12.1
f	Overpressure shift 240 kPa	9.1	9.8
g	Prolonged handling upto 10min	9.2	9.8
h	After cooling	9.6	10.1

Dependence of the solder thickness

In comparison to the previous investigations described in beginning of section 6.3 performed with 150 µm solder thickness, the resulting void percentage in case of solder height of 20 µm and 60 µm was significantly higher. After the increase of the pressure to 240 kPa, the void content was effectively reduced to less than 10 %. However, in spite of the overpressure the void content continued to increase during the following 600 seconds. This resulted in a void content of about 20 % at the beginning of the cooling phase. The solidification of the solder was also much more prominent than with conventional soldering. Both observations could be explained by the much thinner solder gap and speckled connection of IMP between chip and substrate. Thus a much less amount of gas needed to increase the size of a void, and the voids can no longer grow in height but only horizontally. Figure 87 shows the integral image at various points of the TLPS profile [149]. It can be observed that the voids after cooling are dependent mainly on the initial voiding characteristics during solvent burnout. Even after an optimized profile with combined vacuum and overpressure, the uncovered areas with presence of organic residues played a major role in the final void content.

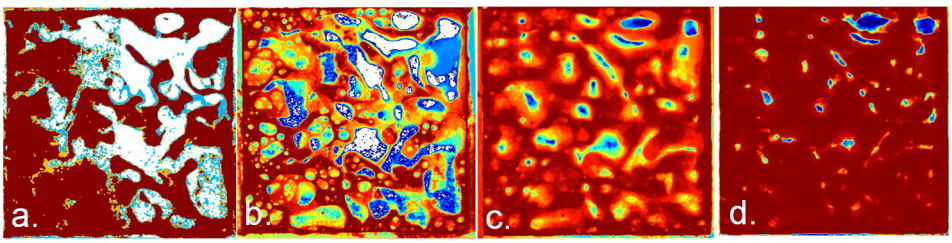


Figure 87: Integral overlay images of TLPS joint at a. during the solvent burnout; b. before solder melt; c. after solder melt; d. end of the profile.

In-situ investigation for preform interlayer

A preliminary analysis on the preforms under in-situ X-ray setup revealed that the wetting characteristics are comparatively better than paste-based TLPS joints. The main reason was the absence of the solvent or flux materials. The tested TLPS profile with combination of vacuum and overpressure for preforms resulted in very high void percentages. This can be attributed to oxidized Cu substrate and improper wetting of molten solder. The main influential factor in this case for a low-void TLPS joint is the proper wetting of the molten metal to chip and substrate surfaces. Figure 88 shows an in-situ recording of a Sn-Cu preform on SPC substrate with roughness $R_z \leq 5\mu m$. It can be observed that the vacuum had no influence on the melt. However an overpressure shift changed the void profile due to pressurized environment eventually pressing the chip from all sides reducing the void percentage.

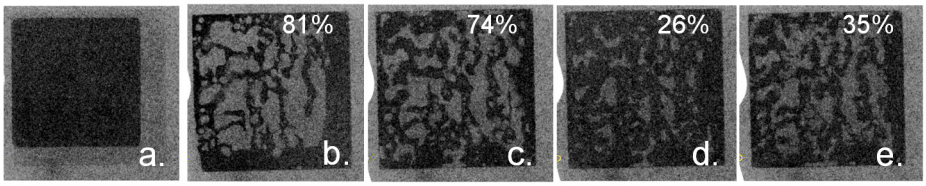


Figure 88: In-situ X-ray recording with variation in voids for a TLPS profile for DCB with R_z of 16 µm and a solder preform at: a. chip placement; b. solder melt; c. vacuum -60 kPa; d. overpressure 240 kPa; e. after 10 min peak time and cooling.

6.4 Conclusion

In this chapter, initially the simulations were performed for estimating the IMP thickness for various profiles with temperature and handling time. The goal was also to check if the IMP growth was similar for different profile variants. Further the VVP and OPC soldering techniques were investigated by the development and modification of profiles for $SnCu_{0.7}$ solder paste after commissioning for power electronic soldering applications. These were supported by the in-situ investigation for paste and preform interlayer materials. In this chapter, the TLPS approaches A1 and B1 were focused for optimizing the process parameters with respect to the pressure changes, peak temperature and time.

The following conclusions are interpreted from this chapter:

- It was concluded from the concentration gradient simulations, that the IMP formation estimation helped in defining the required process time and temperature.

- From the simulations and preliminary analysis, it was observed that temperature profiles with prolonged post-handling at higher temperatures i.e. 260 °C have same IMP growth with prolonged post-handling at lower temperatures i.e. 210 °C below liquidus temperature of the interlayer.
- The IMP formation evidently was higher for peak temperature 280 °C than 260 °C irrespective of the profile time.
- The time required for the IMP growth of 15 µm bondline with copper from both sides of tin material was estimated by the simulation values at approximately 15 min. For one-sided copper availability, peak time of 25 min was estimated.

For the verification, assemblies were built and the IMP growth was measured. The investigated VVP and OPC soldering with void reduction mechanisms mainly vacuum and over-pressure were customized for various materials combinations and the void percentages were also summarized.

- By using vacuum or overpressure as void reduction technique, void percentages less than 5% were achievable irrespective of solder compositions. This holds true for thicker solder heights above 100 µm.
- The solder height and surface properties were the most influential factors in the final void percentage for standard profiles of peak time.
- For thin solder deposits, the surface properties, component sizes and component metallization influenced the void percentages.
- A multiple vacuum profile resulted in better quality compared to stepped or single vacuum profiles.
- Similarly, a multiple SRSF resulted in better quality compared to single SRSF. Here the time to first pressure change, pressure gradients and hold time at peak temperature are main factors to be modified.

Finally the profiles were tested in in-situ set-ups to understand and investigate the idea of combined vacuum and overpressure profile.

- The types of voids observed were the voids due to flux burn out and voids mainly due to tin usage in case of prolonged profiles.
- The roughness of the substrate had significant influence on the initial voiding characteristics, but had no to less influence on the final void percentages.
- The outgassing was easier and resulted in faster void drop in case of smoother surfaces compared to rougher surfaces.
- For prolonged profiles, the roughness of the substrate resulted in increased void size and new micro-voids over the whole interconnect area.

- The growth of the void for thinner solder joints was not anymore horizontal but lateral i.e. parallel to the interfaces.
- The preforms followed irregular melting characteristics i.e. spontaneous melting at the peak temperature and improper spreading and wetting of the components.
- The combination of vacuum and overpressure displayed excellent results for standard and prolonged TLPS profiles.

The interpretations and the results from the extensive analysis for void-free thin solder layers and the in-situ tests are further considered in the process optimization for VVP, OPC and CFL soldering techniques.

7 Production and Characterization of TLPS Interconnects

This chapter gives an overview of the optimization of the present state-of-the-art soldering techniques for diffusion soldering, in particular for TLPS with enhancements in process conditions to reduce the void percentages in the interconnections and at the same time accelerate the rate of IMP formation. Addressing the difficulties in realizing a void-free TLPS joint in large-area die-attach in power electronics, the variations in soldering process parameters like temperature, pressure and time are discussed. The complete transformation of thin Sn-Cu solder interlayers (15-20 µm) into Cu_6Sn_5 IMP and related void information for varying solder profile variants have been explained. To evaluate the feasibility for TLPS process, the void reduction mechanisms and their combinations have been investigated and summarized. An optimized profile has been introduced capable of realizing TLPS joints.

7.1 Process Optimization for Reliable TLPS Interconnects

A comprehensive analysis was performed on the reflow soldering techniques to evaluate and explore the potential for void-free TLPS joints. Here the semiconductor components were soldered onto SC DCB substrates with $R_z \leq 16$ µm using type 6 $Sn_{99.3}Cu_{0.7}$ solder paste. As introduced in section 4.2, the soldering machines used in the module construction were a vapor phase soldering machine capable of vacuum down to 20 mbar during peak time (IBL VAC645) and a reflow convection soldering machine capable of building over-pressure up to 5 bar (relative) in peak temperature chambers (Seho MaxiReflow HP). The profiles tested are shown in Table 27

7.1.1 VVP and OPC Soldering Techniques

As described in section 6.2.2 that the extended profiles with peak temperature had relatively large void percentages. Though the initial void formation started with the flux burn out, the increase in size of the voids and formation of micro-voids was due to the tin consumption for IMP formation. It can be observed in the profiles that a vacuum step was activated at the end of the profile was not influential. The cross-sections showed a

skeleton structure formation due to the standalone Cu_6Sn_5 scallopial structures formed from top and bottom boundaries of the interlayer. Similar skeleton structures were observed due to improper wetting of LMM tin and HMM Cu particles in interlayer in case of composite solders and lateral flow approach, as also described by Ehrhardt et.al. [132; 141].

To reduce the voids formed due to the flux burn-out, an intermediate vacuum step was activated by modifying the profile into two steps, where the first step follows a standard soldering profile to reduce the voids to a minimum and the second step to accelerate the IMP formation further. In this study, four basic variations with peak temperature (T_P) and post-thermal treatment temperature (T_{pt}) in solder profiles were tested, to observe the changes in solder connections with void percentage and IMP formation. The profiles vary in T_{pt} of the soldered joints, i.e. treatment above melting point of the solder (variant a) and below the melting point (variant b) as shown in Figure 88. The profiles P1a and P1b were performed with VVP soldering (2x vacuum at 0.02 bar) with T_{pt} at 260 °C and 210 °C respectively. And the profiles P2a and P2b were performed with high-pressure convection soldering (2x SRSF at 5 bar) with T_{pt} at 260°C and 210°C respectively. In all the profiles, the extreme parameter settings of the machines with temperature and pressure were used.

To observe the influence of process parameters such as peak time and pressure variation, a statistical analysis was performed to assess the void percentages. As explained in the preliminary void analysis section 6.3, one normal reflow with 1x vacuum is taken as Standard Vacuum (SV) and with 1x SRSF cycle as Standard high-pressure or overpressure (SH). For above mentioned profiles, the time of post thermal treatment (t_{pt}) was extended from 5 to 20 minutes in steps of 5 minutes for each case of P1 and P2 variants as shown in Table 27.

A basic explanation is as follows:

P1a_SV: Standard profile with T_P=260°C and 1x vacuum.

P1b_2xSV+10: Standard profile with two vacuum cycles with T_P=260°C and T_{pt}=210°C for t_{pt}=10 min.

P2a_SH: Standard over-pressure profile with T_P=260°C and 1x SRSF.

P2b_2xSH+5: Standard over-pressure profile with two over-pressure SRSF cycles with T_P=260°C and T_{pt}=210°C for t_{pt}=5 min.

Same methodology can be followed for understanding the mentioned profiles in Table 27 and for Figure 89.

Table 27: Overview of the tested profile variants for VVP and OPC soldering for post-handling temperature and time.

Variant **P1**	Profile name	P (bar)	Variant **P2**	Profile name	P (bar)	T_P (°C)	T_{pt} (°C)	t_{pt} (min)
P1a	SV	0.02	P2a	SH	5.0	260	-	-
P1a	2xSV	0.02	P2a	2xSH	5.0	260	-	-
P1a	2xSV+5	0.02	P2a	2xSH+5	5.0	260	260	5
P1a	2xSV+10	0.02	P2a	2xSH+10	5.0	260	260	10
P1a	2xSV+15	0.02	P2a	2xSH+15	5.0	260	260	15
P1a	2xSV+20	0.02	P2a	2xSH+20	5.0	260	260	20
P1b	2xSV+5	0.02	P2b	2xSH+5	5.0	260	210	5
P1b	2xSV+10	0.02	P2b	2xSH+10	5.0	260	210	10
P1b	2xSV+15	0.02	P2b	2xSH+15	5.0	260	210	15
P1b	2xSV+20	0.02	P2b	2xSH+20	5.0	260	210	20

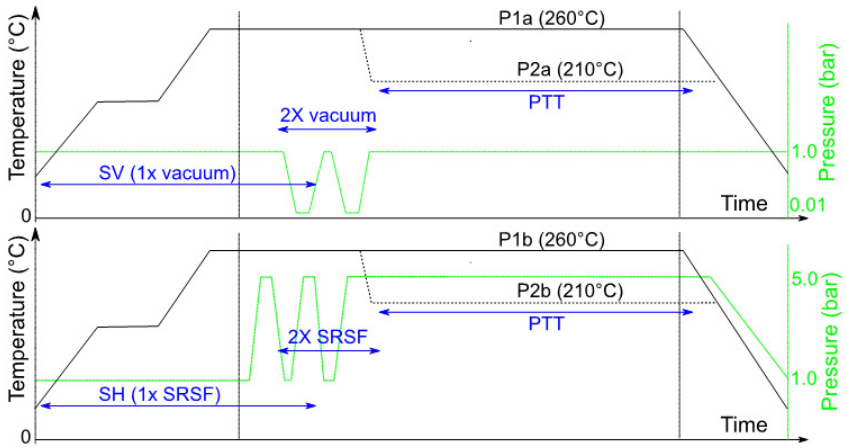


Figure 88: Profile variation with pressure cycles and time for the thermal treatment of the assemblies as introduced in Table 27.

For the void and IMP analysis, the profiles were tested for components with varying sizes as introduced in section 4.3. The power semiconductor components resistor-chips (2.3mm x 2.3mm), diodes (9mm x 8.5mm), transistors (15mm x 8mm) with standard Ni/Ag bottom-side metallization were soldered to SC DCB substrates. For each variant, 6 resistors, 3 diodes and 2 transistors were used for soldering process and further evaluation. An overview of the void percentages with the specified profiles is given in Figure 89. A double reflow either with vacuum or over-pressure lead to a solder joint with better results, as the second pressure cycle acts on the void content from the first cycle. The probability of new void formation is relatively low due to higher usage of flux in first step of profile to deoxidize the copper surface of the substrate.

Void Analysis

It can be observed in Figure 90.a-d, how the void percentage varies with prolonged post thermal treatment. Most of the bigger voids had been removed with the double over-pressure or double vacuum profiles, but upon extended heat treatment, smaller voids could be seen and these increased in size with time. The components with smaller dimensions i.e. resistors showed relatively lower voids in comparison to bigger components i.e. IGBTs or diodes.

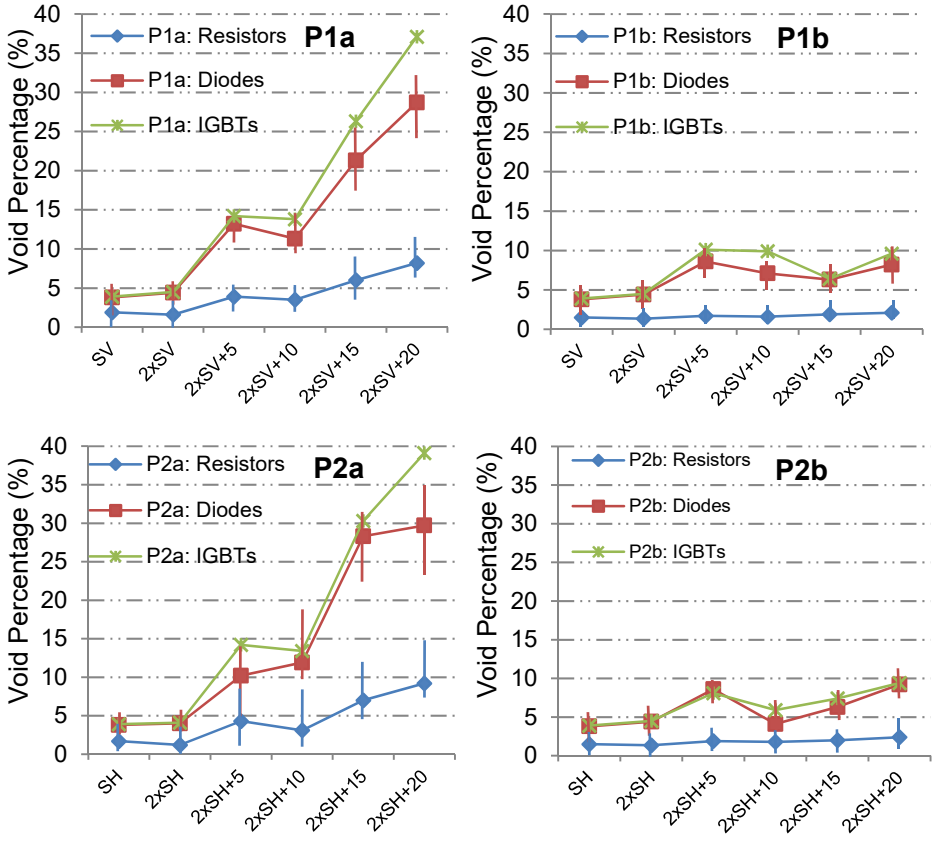


Figure 89: Void percentages for profile variants P1a, P1b, P2a and P2b with prolonged post-thermal treatment with respect to void-reduction technique. Here n = 6 for resistors; 3 for diodes; 2 for IGBTs.

It was observed that for all profiles, reduction in void percentage was seen at tpt=10 min, clearly observed for over-pressure profiles. An explanation for such fluctuation could be the compression effect of the built over-pressure leading to settling of parent materials as the rest fluidic tin is slowly

used for the phase transformation. This accelerates the phase formation rate along with temperature and time while keeping the void content to minimum. The graphs for both variants show that the void percentages stay under a certain level for T_{pt}=210 °C irrespective of time increase. As seen in Figure 89.a-d, the voids dropped for T_{pt}=260 °C, t_{pt}= 10 min for both over-pressure and vacuum profiles. But occurs at T_{pt}=210 °C, t_{pt}=10 min for over-pressure and at t_{pt}=15 min profiles showing that high pressure is more influencing for IMP formation. An overview of the X-ray images for the selected profiles is given in sub-chapter 7.2.

IMP Analysis

The samples from the above specified profiles were also used in IMP assessment through cross-sectional analysis. In Figure 90 and 91, the cross sections of selected samples are shown for varying Tpt and tpt with 2x pressure cycles. It can be seen in Figure 90a that in VVP profiles, P2a_2xSV+5 with the treatment at T_{pt}=260 °C, rest tin from the solder material can be seen for t_{pt}=5 min. For P2a_2xSV+15 at t_{pt}=15, the solder layer is completely transformed into Cu_6Sn_5 IMPs. Different reaction kinetics could be seen where only 3µm of IMP was formed leaving >10µm rest tin for T_{pt}=210 °C. For joints with P2b_2xSV+15: T_{pt}=210 °C and t_{pt}=15 min, similar structures can be observed as in joints of P2a_2xSV+5 with T_{pt}=260 °C and t_{pt}=5 min. It can be observed from Figure 90 that parameters T_{pt}=260 °C and t_{pt}<15 min were sufficient to transform 90% of the solder joint into Cu_6Sn_5 IMP. For a full IMP transformation, a higher PTT was required at 25 min with a total profile time of 33 min.

The cross-section images as shown in Figure 91 for overpressure profiles indicate better IMP formation with different reaction kinetics compared to the vacuum profiles. A prolonged peak time t_{pt}=15 min at 260 °C, transformed the interlayer completely into IMPs, but with void percentages >25% for larger components as seen in Figure 89, which impairs the thermal and electrical properties of the joint. The profile P2b_2xSH+15 with T_{pt}=210 °C and t_{pt}=15 min also transformed completely the solder layer into Cu_6Sn_5 IMP with voids less than 10% for diodes and transistors and less than 3% for resistors. In other profiles with low PTT time or low PTT temperature, rest tin was always observed in all the cross-sectioned samples.

The same profile exhibited a faster IMP formation rate for Cu-dummies as shown in Figure 92a similar to reaction kinetics and IMPs in Cu/Sn/Cu system. It can be observed for the same profile, the availability of Cu from Cu-dummy and DCB substrate into liquid Sn was higher, resulting in thicker Cu_6Sn_5 and Cu_3Sn phases.

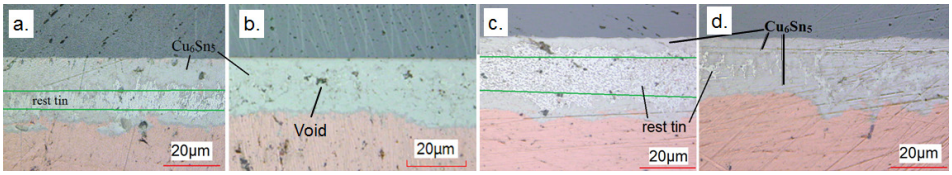


Figure 90: Cross-sections of variants with 2xSV a. P1a with T_{pt}=260 °C and t_{pt}=5 min; b. P1a with T_{pt}=260 °C and t_{pt}=15 min; c. P1b with T_{pt}=210 °C and t_{pt}=5 min; d. P1b with T_{pt}=210 °C and t_{pt}=15 min.

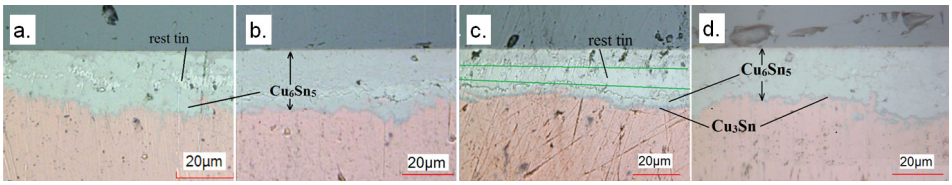


Figure 91: Cross-sections of variants with 2xSH: a. P2a with T_{pt}=260 °C and t_{pt}=5 min; b. P2a with T_{pt}=260 °C and t_{pt}=15 min; c. P2b with T_{pt}=210 °C and t_{pt}=5 min; d. P2b with T_{pt}=210 °C and t_{pt}=15 min.

Upon preliminary analysis with 2.3 mm x 2.3 mm components, the joints showed shear values of greater than 54 N/mm2, but the defect code was mainly component break or interfacial delamination. The shear values with Cu dummies showed 68 N/mm2. The solder profile P2a_2SH+20 with T_{pt}=260 °C and t_{pt}=20 min resulted in IMP formation to more than 30 µm as in Figure 92b, but with higher void content which needs to be optimized in case of solder interlayers. The evaluation of mechanical properties with the selected profile variants and further optimization of TLPS process for reliability tests are continued in section 7.3. A combination of vacuum and over-pressure in same solder profile is not yet possible in the state-of-the-art vapor-phase or convection reflow ovens. This could result in excellent results as summarized in section 6.3.2 of in-situ analysis. The combination of such profiles and machine development has to be investigated by the reflow machine manufacturers.

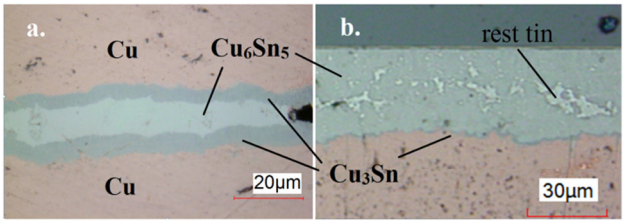


Figure 1: Comparison of IMP formation in Cu/Sn/Cu system and Si/Sn/Cu system for the profile P2a_2SH+20.

7.1.2 CFL Soldering Technique

The heat transfer mechanisms and the corresponding void and IMP analysis lead to the conclusion that the IMP formation is also dependent on the type of heat transfer used as it directly correlates the energy transfer for the activation of diffusion. The formation of the IMPs also depends on the process gas used during the process, as this ensures high quality surfaces during diffusion. In case of VVP soldering, the energy transfer is intensive but at atmospheric pressure. In case of OPC soldering, the energy transfer is comparatively low to VVP, however the usage of over-pressure ensures void reduction and accelerated the IMP formation at the same time. As tested in case of preliminary IMP analysis in sub-chapter 6.2, the heat transfer plays also a major role and the position and direction of the heat application as well. Further analysis in case of heat transfer mechanisms is summarized in section 7.1.3.

The testing of CFL soldering was done with the profiles as shown in Figure 93. To check the IMP formation and voiding, four preliminary profiles were chosen with peak and post-handling times at temperatures of 260 °C and 210 °C as shown in Table 28. The post-handling treatment was extended to maximum of 20 min in each case. Theses profiles were considered based on the investigations from the VVP and OPC soldering. The CFL machine at Pfarr Stanztechnik Gmbh, Buttlar was used and further analysis of the assemblies was performed at Institute FAPS. Here the substrates bare Cu- SPC and Ni- plated SNC DCB substrates with $R_z \leq 5$ µm were used. The preforms and components were placed manually on the substrates and CFL soldered.

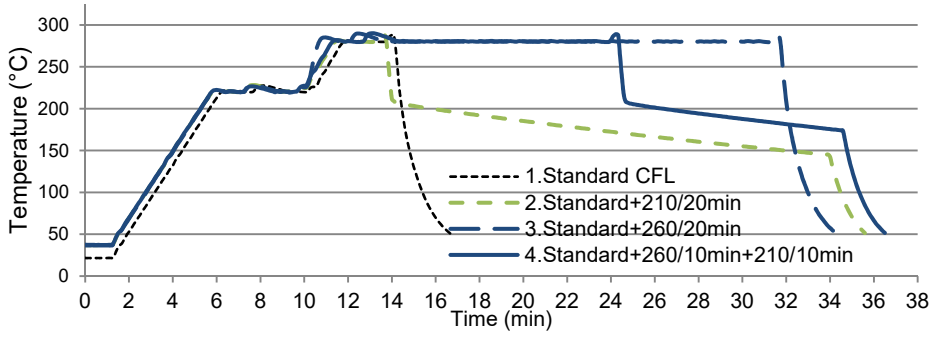


Figure 93: Tested temperature profiles for the preform-based TLPS with varying peak and post-handling times at 260 °C and 210 °C respectively.

Table 28: Tested CFL profiles for evaluation of IMP growth in various preforms.

Profile Nr.	Peak temperature (°C)	Peak time (min)	Post-handling temperature (°C)	Post-handling time (min)
1	260	3	-	-
2	260	3	210	20
3	260	3	260	17
4	260	10	210	10

With the tested profiles, the Cu-DCBs had best results for IMP formation. Ss introduced in sub-chapter 5.3, the preforms were in this case were B1P1 and B1P2 of thickness 25µm and cladded preforms B2PC of 75 µm. In case of B2PC cladded preforms, the copper inlay in the preform is expected to be used in the IMP formation from middle of the bond-line resulting in full transformation into η phases in shorter time compared to thin preforms B1P1 and B1P2. The initial voiding results of the used preforms with profile 1 were already introduced in sections 5.3 and 6.3.1. Figure 94, 95 and 96 show the cross-sectional images of various preforms and substrate metallization combinations for the profiles 2, 3 and 4 respectively. It can be observed that the preforms had a relatively good IMP formations in case of B1P1 (Sn-Cu) and in some cases B1P2 (Sn-Cu-Ni) preforms with full transformation in the bondline. But this held true only for the Cu-DCBs due to abundance of available copper. The cross-sections show that the IMP formation was not complete in bondline even in case of cladded preforms on Ni plated surfaces. This can be attributed to the formation of Ni_3Sn_4 IMPs parallel to Cu_6Sn_5 IMPs. It can be clearly observed that the presence of Ni hinders the formation of Cu-Sn IMPs in both cases with B1P1 or B1P2 preforms on Ni-DCBs. However this is not true for Cu-DCBs as no Ni_3Sn_4 IMPs were observed irrespective of the preform type.

Similar to the IMP thicknesses in the analysis of Cu-Sn paste based TLPS in section 6.2, the IMPs had thicknesses according to the PTT temperature and time. In Figure 94, with a PTT even 20 min did not transform the bondline into IMPs on Cu-DCBs. The scallopial structures of approx. 4 µm were observed. An IMP thickness of approx. 10 µm were formed due to availability of copper from the preform in B2PC preforms. The bottom side of preform on Ni-DCB showed no IMPs due to Ni-plating.

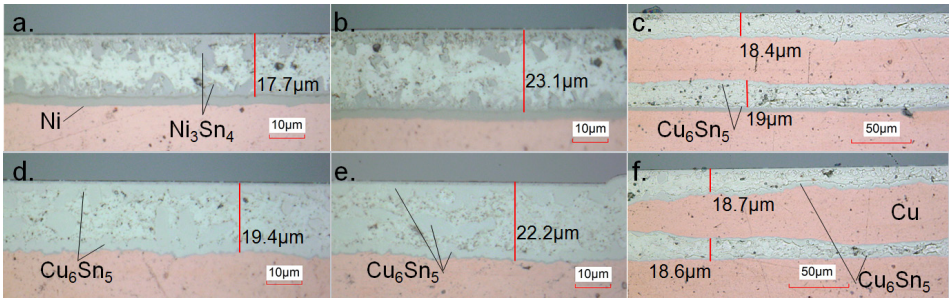


Figure 94: Cross-section images of the soldered assemblies with profile 2: standard CFL + 210°C-post handling for 20 min. a. B1P1, b B1P2, c.B2PC on Ni-DCB; d. B1P1, e. B1P2, f. B2PC on Cu-DCB.

In Figure 95 with a total PTT of ~20 min of profile 3, in case of Cu-DCBs, a full transformation into Cu_6Sn_5 IMPs was observed. Only in case of B1PC cladded preforms, a full IMP was possible on both Cu- and Ni-DCBs due to abundance of copper from cladded copper inlay.

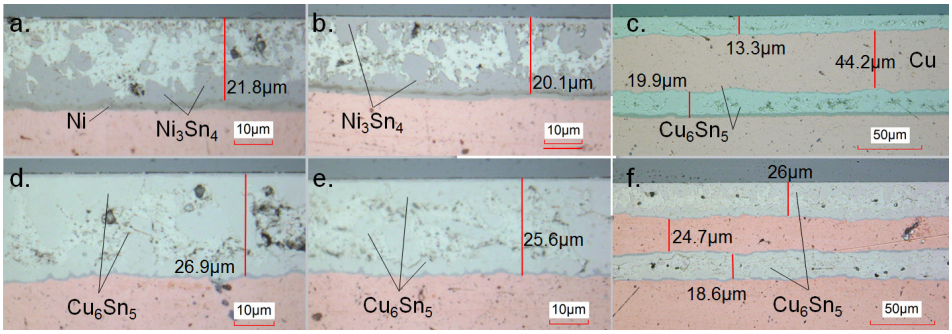


Figure 95: Cross-section images of the soldered assemblies with profile 3: standard CFL + 260°C post handling for 20 min. a. B1P1, b B1P2, c.B2PC on Ni-DCB; d. B1P1, e. B1P2, f. B2PC on Cu-DCB

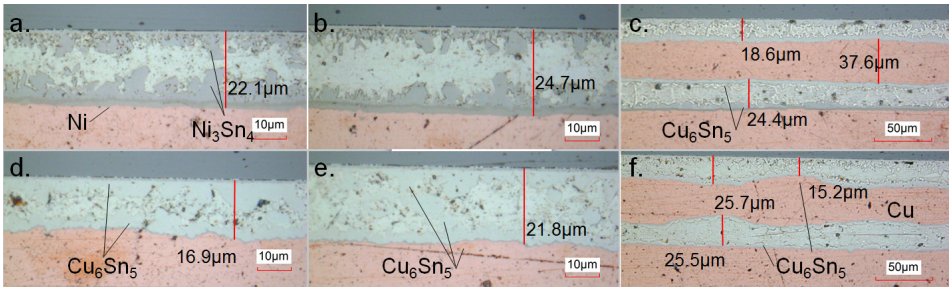


Figure 96: Cross-section images of the soldered assemblies with profile 4: standard CFL + post-handling at 260°C for 10 min and at 210°C for 10 min. a. B1P1, b B1P2, c.B2PC on Ni-DCB; d. B1P1, e. B1P2, f. B2PC on Cu-DCB.

The profiles with 210 °C post-handling temperatures had relatively low void percentages at 2% compared to prolonged PTT of 20 min at 260 °C at 4.5%. For Ni-DCBs, the Ni_3Sn_4 IMPs increased in size consuming the Ni- plating on the substrate.

From Figure 96, it can be observed that rest tin was always seen in bondlines on both the substrate types. However, it must be noted that a full-IMP bondline was observed in case of B2PC and Cu-DCB combination with just PPT of 10 min at 260 °C and 210 °C. It can be observed also from the Table 29, that the IMPs dominated mainly on the availability of the copper for diffusions. Though both the IMPs Cu_6Sn_5 and Ni_3Sn_4 had similar activation energies, the Ni presence definitely influences the final bondline structure. Further crucial factor was the copper in the interlayer that the IMP Cu_6Sn_5 and Cu_3Sn formation dominated irrespective of the preform type or substrate. Due to presence of Ni in B1P2 preform, the Cu_3Sn IMPs were not observed as in B1P1 or B2PC preforms.

Table 29: Overview of the observed IMPs in the substrate and preform combinations for the profile 3 and 4.

Substrate/ Preform	B1P1 (SnCu)	B1P2 (SnCuNi)	B2PC (Sn-Cu-Sn)
SPC (Cu-DCB)	Cu_6Sn_5, Cu_3Sn	Cu_6Sn_5	Cu_6Sn_5, Cu_3Sn
SNC (Ni-DCB)	Ni_3Sn_4	Ni_3Sn_4	Cu_6Sn_5

After the extensive analysis, the soldering profile as shown in Figure 98 was chosen and finalized according to the intended void percentages or material combinations. In case of Ni based preforms B1P2, the profile with Tpt of 210 °C for 30 min was considered to reduce the final voiding. In case of preforms B1P1 and B2PC, the profile with 260 °C peak temperature for 25 min was considered to ensure full IMP transformation. The profile also shows the combination multi-vacuum and overpressure cycles that were modified to achieve lowest void percentages. Here an excellent quality of the TLPS joints was obtained due to preliminary formic acid treatment of the materials followed by the soldering under forming gas and nitrogen. The settings of the CFL soldering were vacuum down to 0.01 bar and over-pressure with fluctuations up to 1.2 bar. Supportive spring structures were used in the soldering jigs to accelerate the IMP formation in the bondlines.

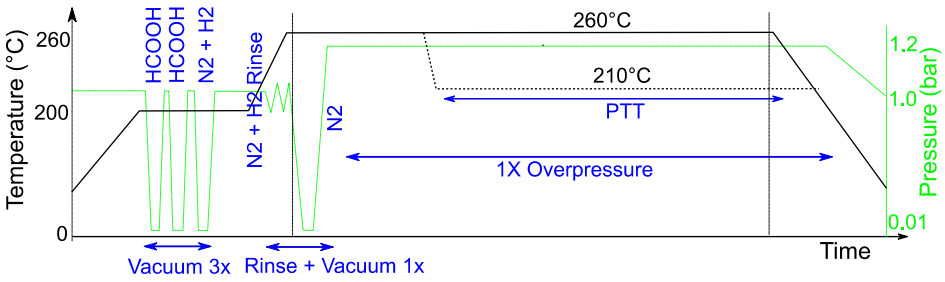


Figure 97: Finalized temperature profile for the production of TLPS joints through CFL soldering.

7.1.3 Comparison of the Soldering Mechanisms

The heat transfer mechanism had a great influence on the produced interconnects mainly in case of IMP formation and the void formation. This can be named according to the test setup used in the experiments as:

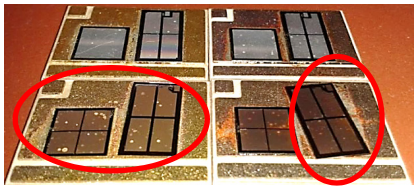
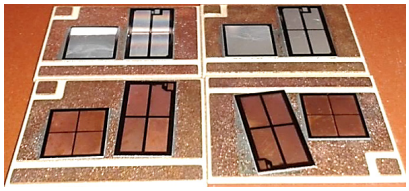
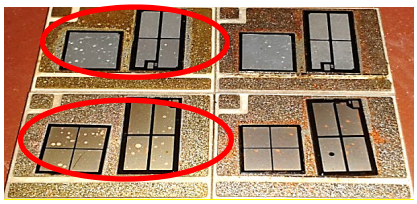
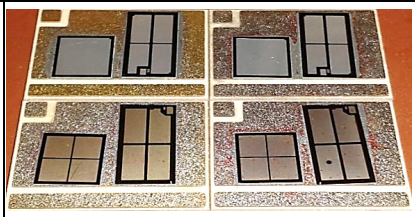
1. Low mechanical pressure-assisted heat transfer (in VVP and CFL soldering)
2. Overpressure assisted heat transfer (in OPC soldering)

The influence of over-pressure in the hyper pneumatic chamber during the complete peak time accelerated the IMP formation rate compared to vapor-phase soldering. A multiple pressure cycle at critical points (SRSF) of the temperature profile immensely reduced the voids to < 5% even for prolonged reflow profiles of 30 minutes with varying post-thermal treatment. It can also be concluded that, the profile with higher over-pressure levels (e.g. 5.0 bar instead of 3.0 bar) with Tp below melting point of interlayer had better results. Though VVP soldering had advantages with void reduction, high-pressure soldering emerges as a dominant mechanism for both void reduction and IMP formation at the same time. The CFL soldering resulted in high quality TLPS joints with low defects of < 2% voids in case of B1P1 and B2PC preform on Cu-DCBs and full IMP transformation.

Depending on the peak- and post-handling time of the VVP soldering, the test assemblies mainly the semiconductors were affected by the aggressive condensation medium leaving residues on the components as shown in Table 30. This was higher in case of assemblies with post-handling at 260 °C (before cleaning, left) compared to the assemblies with 200 °C post-handling observed on both types of metallization. It can be seen that all the DCBs were oxidized irrespective of the temperatures, as this happens only during the cooling phase in normal atmosphere after decondensation. A post-cleaning step of atleast 20 min was required for further wire-bonding

process. The water-based cleaning agent (VIGON N600) showed good results on both types of metallizations and DCB surfaces. In case of solvent-based cleaning agent (ZESTRON FA+), residues were observed on components and DCB surface.

Table 30: Overview of substrates for the profiles with peak-temp./post-handling of assemblies with 260°C/260°C and 260°C/200°C respectively.

	Before cleaning	After cleaning
1. Water-based cleaning agent		
2. Solvent-based cleaning agent		

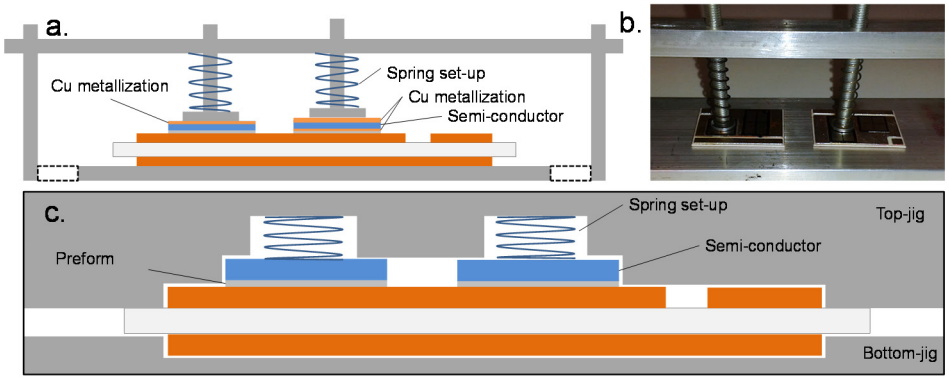


Figure 98: Opted solution for the soldering of the copper metallized components to avoid warpage (top; a,b); for the preform-based soldering to accelerate the IMP growth for all types of components (bottom; c).

Compared to the VVP soldering, the OVP soldering had residues on the components, but the copper surfaces on both Cu-metallized components and DCBs were oxidized, as the OPC soldering was performed with normal air i.e. not under inert gas nitrogen. For both VVP and OVP soldering of copper metallized components, a work piece carrier with spring structures as shown in Figure 98 was opted to reduce the warpage. The assemblies

from the CFL soldering had high surface quality, as the substrates were under process gas until cooling down to room temperature. Here custom modified graphite jigs were used for accurate placement of preforms and components and homogenous energy transfer to the assemblies. The assemblies were sent to wire-bonding without need of any cleaning step in case of CFL soldering. The developed demonstrators as part of the thesis using VVP and CFL soldering are shown in Figure 99.

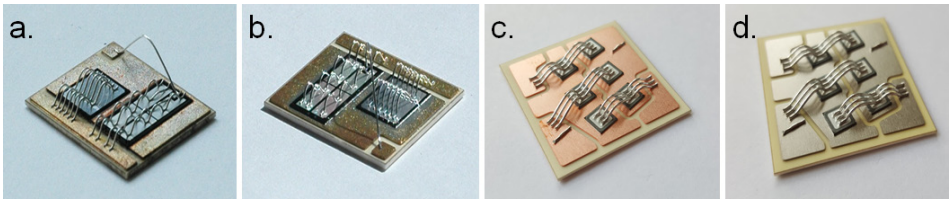


Figure 99: Demonstrators showing the implemented TLPS die-attach: IGBT/Diode assemblies with VVP soldering a. 260°C/260°C, b. 260°C/200°C; multichip diode assemblies with CFL soldering c. Cu-DCB, d. Ni-DCB.

7.2 Influences of Materials in the TLPS Process

This sub-chapter focuses on the explanation of various influences and defect formations in TLPS interconnects according to the component metallization, substrate materials and interlayer compositions.

7.2.1 Chip Metallization

The chip metallization had a major influence on the bondline formation, IMP growth and void percentages. In case of the copper metallization, the CTE mismatch between different layers of the component i.e. frontside copper, silicon and in few components backside copper was the main reason for the chip warpage. This was observed not only for the TLPS profiles, but also for conventional solder profiles. This was however also interdependent on the interlayer thickness under the chip. In case of components with standard NiAg and Al metallizations, the influences were comparatively less i.e. less warpage and homogenous bondline. Figure 100 and Figure 102 show the 3D-profiles of the copper metallized components for VVP solder profile at 260 °C with peak time of 2.5 min for solder layer thickness of 60 µm on SPC substrates ($R_Z \leq 5$ µm). It can be observed that the frontside thicker Cu-metallization had significant influence on the chip-warpage and void formation. Even with vacuum activation down to 15 mbar, the void percentages were over 9 %.

In case of the square shaped 600V IGBT (9.73 mm x 10.23 mm), the copper metallization was thicker up to 80 µm. In Figure 100, it can be observed that the warpage was around 12.5 µm (scan 3) due to local expansion of the copper islands. The void formation was observed mainly at the regions of higher Cu-thickness of 10 - 11 µm (scan 2). For the rectangular shape of the 600V diode (9.2 mm x 5.44 mm) version with top-Cu metallization i.e. ~65 µm also as thick as the silicon material, the maximum warpage observed in vertical direction was 43 µm as seen in Figure 102.

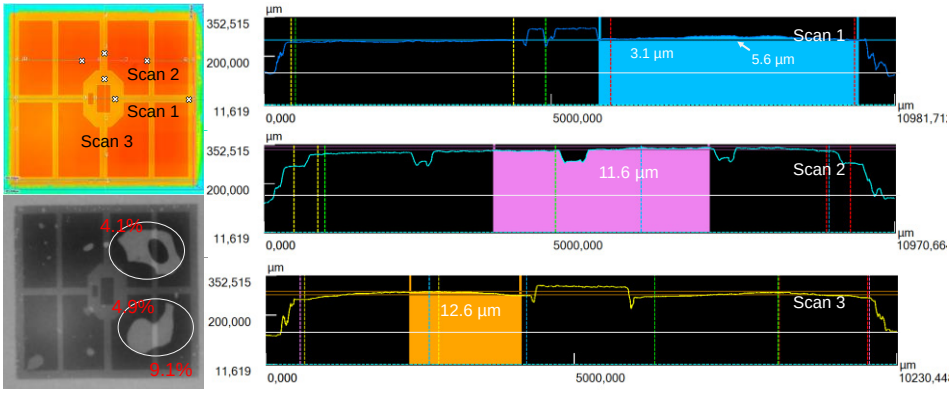


Figure 100: Surface profile analysis of an IGBT with two sided Cu-metallization showing a total warpage of max.12 µm.

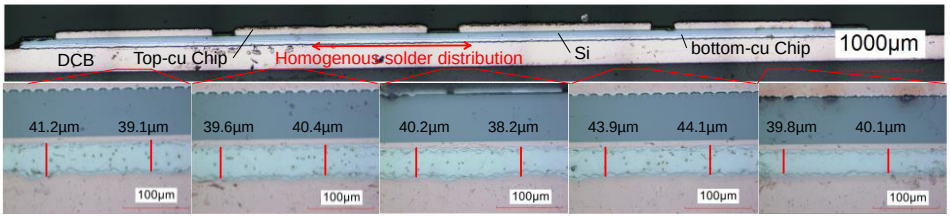


Figure 101: Cross-section of the soldered IGBT with two sided copper metallization with homogenous solder distribution along the complete bondline.

This can be observed also in the cross-section as shown in Figure 101 and 103. The extreme warpage of the diode compared to IGBT can be attributed to frontside Cu-metallization over the entire chip region compared to copper island metallization for IGBTs. Due to the warpage of the components, the solder material was pulled towards the center. Further the warpage characteristics for copper metallized components for profiles with prolonged peak time were analyzed as shown in Figure 104. Here the profiles from section 6.2.2 with peak time of 6 min and 15 min at 260 °C were selected and soldered without the work piece carrier with springs. The

components of both one-sided i.e. one-sided (top) and both-sided Cu-metallization were used. Due to just 7 µm of Cu-layer on the silicon material, warpage was not observed even in case of rectangular components and for printed solder layer thickness less than 30 µm. However large lateral voids in the bondline were seen due to deficit of tin material and higher surface roughness. In case of components with two-sided metallization, the warpage was to the extreme in all the types either square or rectangular shape with copper islands. This was due to the prolonged thermal exposure and expansion of top Cu- metallization.

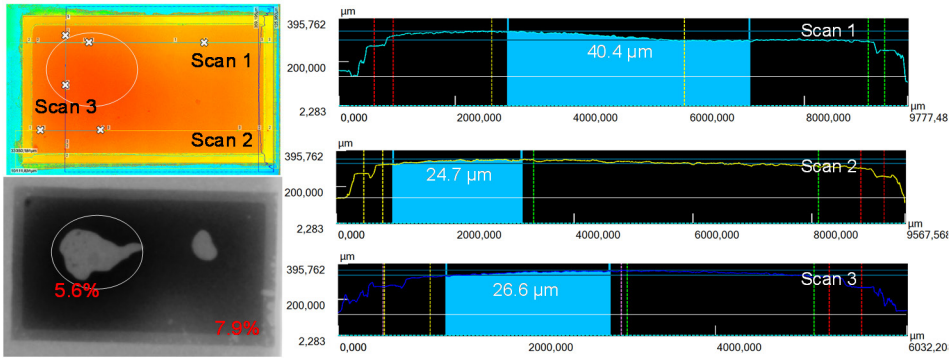


Figure 102 Surface profile analysis of a diode with two sided Cu-metallization showing a total warpage of max. 43 µm.

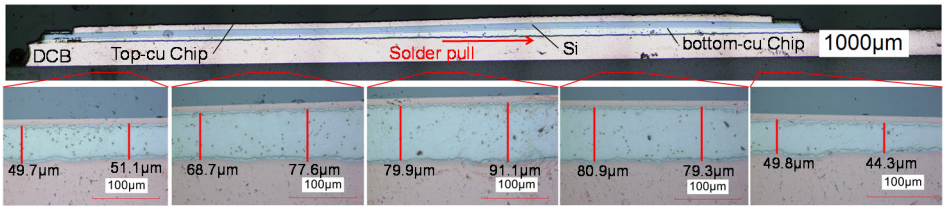


Figure 103: Cross-section of the soldered diode with two sided copper metallization with non-uniform solder distribution and solder pull towards right due to warpage.

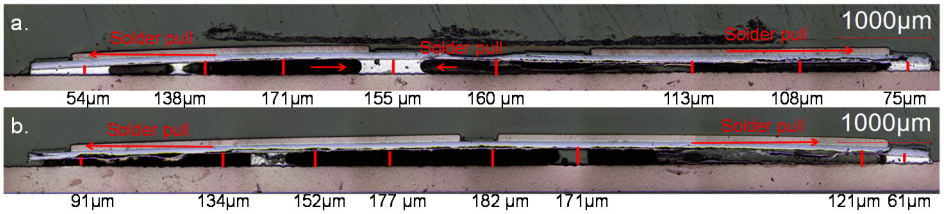


Figure 104: Chip warpage of both-sided IGBT components for the profiles with peak time of 6 min and 10.5 min at 160 µm and 182 µm respectively.

The X-ray images of the components with NiAg/Al metallizations with varying peak temperature and paste materials are shown in Figure 105. This

shows that the void percentages were highest in case of type 8 paste materials. The total voids increased with increasing component size. This can be attributed to the presence of higher fraction of flux materials for printability and comparatively difficult and incomplete outgassing for thinner interlayers. Though the paste application in both type 7 and type 8 pastes was homogenous, the complete chip area was filled with increased arbitrary shaped voids were observed for type 8 solder paste.

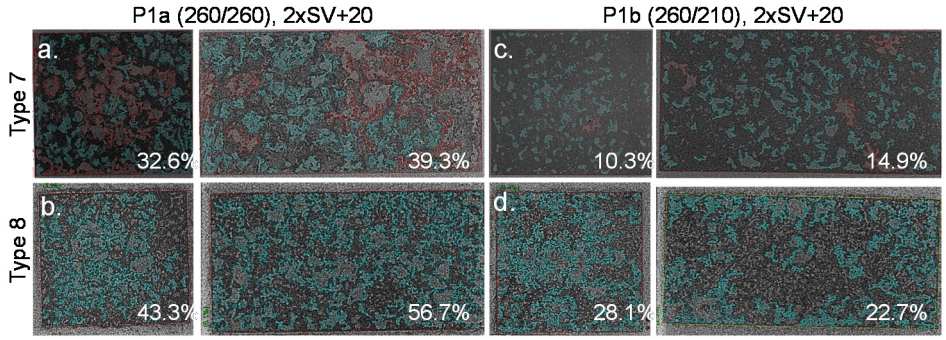


Figure 105: Overview of the X-ray pictures for diodes and IGBTs with 20 µm solder height of paste type 7 for profiles with 20min PTT.

The X-ray images of the components with Cu- frontside metallization with and without spring supports are shown in Figure 106. The warpage of the copper metallized components was extreme even with work piece carriers as seen in Figure 107.c,d. Here a uniform pressure over the chip entire area was required to enable low void TLPS formation. The warpage was high in case of both rectangular and square shaped components with one-sided or two-sided metallizations. It can also be observed that the gap generated due to chip warpage shifted to the positions with less support.

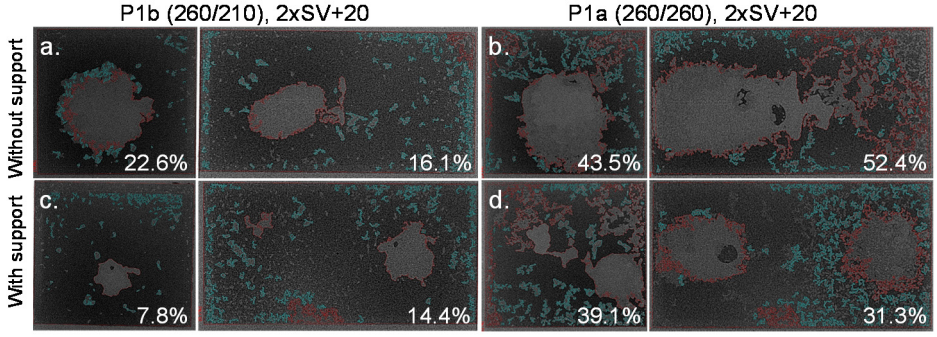


Figure 106: Overview of the X-ray pictures for copper metallized components for a 20 µm solder height in VVP soldering with and without as in Figure 98.

In case of the Ni-plated and bare Cu- DCB substrates, the IMP formation was complete in bondline with selection of the profile parameters as in section 7.1.2. This can be seen in Figure 107 where the preform type B1P1 was used on the substrate variants to demonstrate the preform- based TLPS approach. It can be observed that the void percentages were under 4% due to high quality TLPS technique with multiple pressure cycles and process gases.

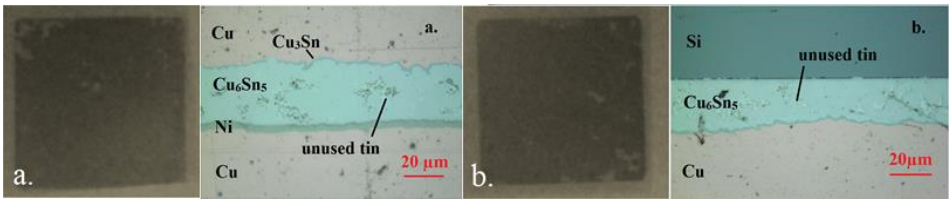


Figure 107: X-ray and cross-sectional images of the preform-based TLPS joints with low-void percentages [151; 186] a. Cu-dummy on Ni-DCB; b. Si chip on Cu-DCB.

In case of Ni-plated DCBs and components with no Cu- frontside metallization, the nickel plating hindered the Cu_6Sn_5 formation in all the cases. An increasing grain size of the Ni_3Sn_4 IMP could be observed in Figure 108, where the Cu-Sn IMPs were completely consumed with increasing peak handling time.

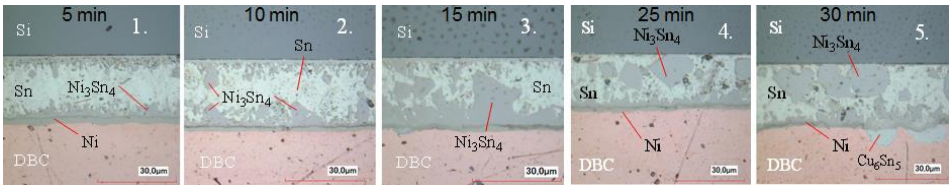


Figure 108: Influence of Ni-metallization in the preform based TLPS approach with increasing peak handling time [151].

7.2.2 Interconnection Medium

The figures 109, 110, 111 and 112 show the X-ray images of various components for VVP and OPC soldering. Only selected images are shown here for the prolonged temperature profiles to discuss the influences. It can be observed from these figures that smaller components had comparatively better void percentages with variation in type of solder paste and profile time. This can be explained due to effective void reduction mechanism in case of smaller surface areas. It can be seen in the Figure 109 and 110 that the profiles with lower post-handling temperatures i.e. 210 °C had significantly lower void percentages as explained in the sub-section 7.1.1.

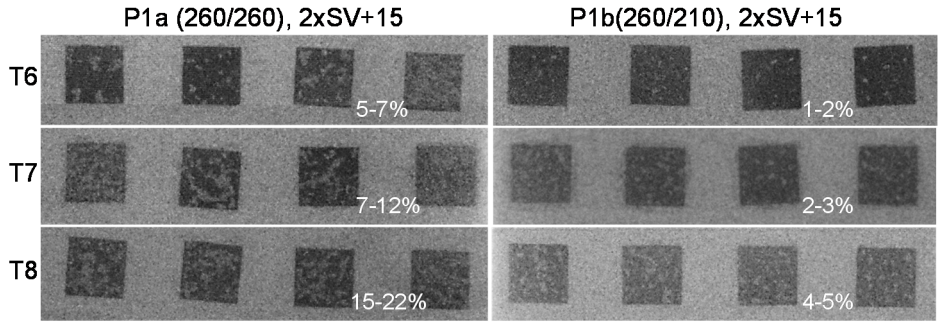


Figure 109: X-ray images of components of 5.3 mm² surface area for VVP soldering with varying solder paste type and post handling temperature.

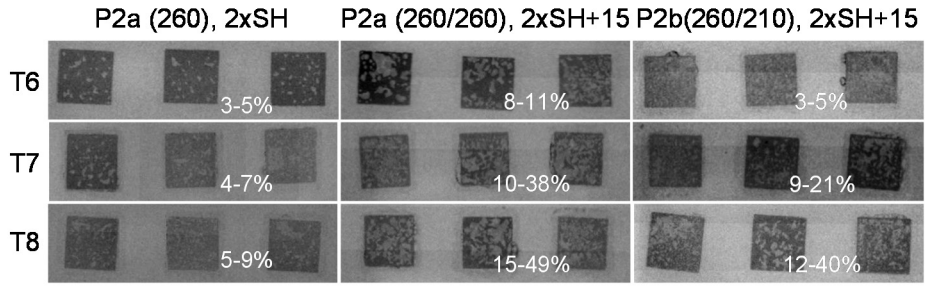


Figure 110: X-ray images of components of 5.3 mm² surface area for OPC soldering with varying solder paste type and post handling temperature.

With either paste type or post thermal treatment at 260 °C, the voids increase exponentially upto ~25%. In case of OPC soldering, the void percentages raised to > 30% due to accelerated IMP formation and tin consumption. Figure 111 gives an overview how the void percentages are affected by the solder height and profile time. The voids were comparatively higher in case of 20 µm interconnects and with prolonged peak time, the voids increased up to 25%. In comparison to type 7 and type 8 solder paste, it can be inferred that type 6 had better final void percentages irrespective of component size due to lower flux content. It can also be clearly observed from the red marked areas, how the voids enlarge laterally in both PTT of 260 °C or 210 °C PTT.

As can be observed from the Figure 112 and Figure 113 of assemblies with OPC soldering for larger components, the interconnects with finer particles and high flux content as in type 8 solder pastes had component offset defects as in Figure 113b,d,f. Similar characteristics of laterally enlarged voids was observed with extended PTT.

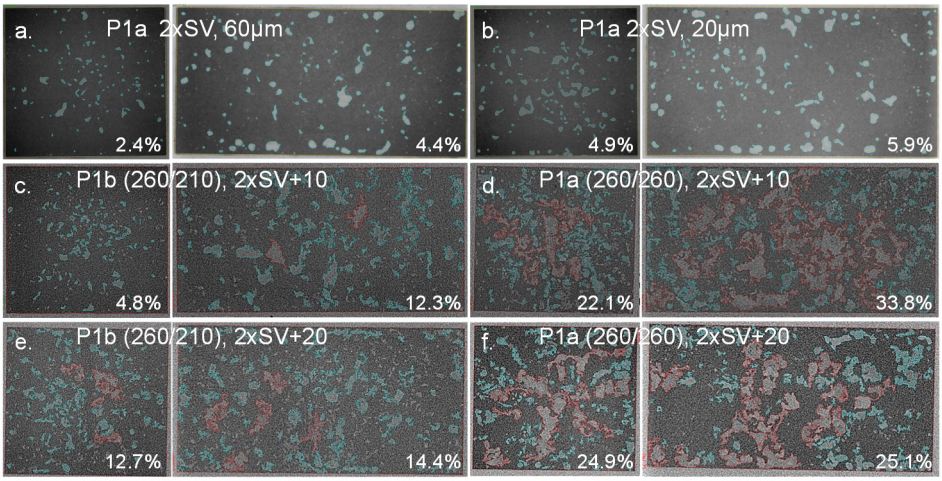


Figure 111: Overview of the X-ray pictures for diodes and IGBTs with type 6 paste from VVP soldering for solder height 60 µm and 20 µm (b - f).

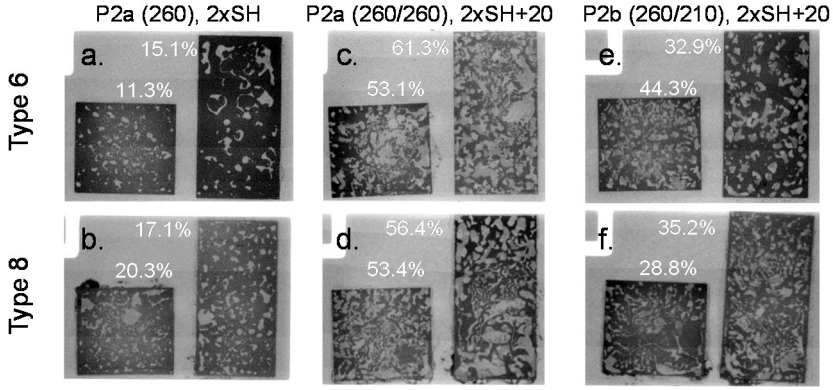


Figure 112: Overview of the X-ray pictures for diodes and IGBTs with 20 µm solder height for the solder profiles 2XSH (a,b), P2a-2SH+20 (c,d), P2b-2SH+20 (e,f) for varying solder paste types.

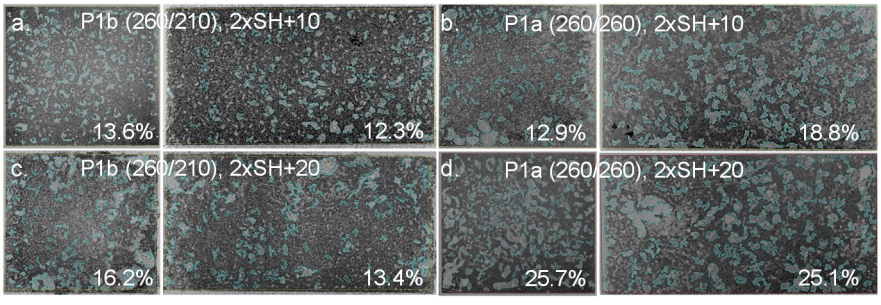


Figure 113: Overview of the X-ray pictures for diodes and IGBTs with type 7 paste of: 20 µm solder height: a. P2a-2SH+10; b. P1a-2SH+10; c. P2a-2SH+20; d. P1a-2SH+20.

Influence parameters in CAPM based TLPS production methodology

In case of interlayers with higher copper mass fraction, different types of voids generally formed in the bondline. These can be interfacial voids or also voids formed from scaffolding or skeleton formation of copper particles. These are usually arbitrary in shape as shown in Figure 114 from the research of project HotPowCon [130; 187] which are fundamentally different from the conventional solder voids. With copper content of 20 - 30 % in the metal portion of the solder paste, a skeleton of copper particles is formed which are connected to one another by IMPs and prevents wetting in the solder gap during soldering producing arbitrary pores. To understand how the copper content influences, experiments were carried out with varying copper content from 0% to 50% in steps of 10% each with varying paste type i.e. from paste type 3 to paste type 6 [187]. The goal was to estimate the amount of copper needed to ensure low-void percentages with no increase in the final chip height after soldering. For this various overpressure profiles were investigated. The results of the void-content and the height difference can be found from the dissertation of Klemm [173] and project report of HotPowCon. It was observed that the void contents stay near to 50% due to the wetting complications. The treatment of the interlayers with formic acid and forming gas together with mechanical pressure however reduced the pore formation significantly.

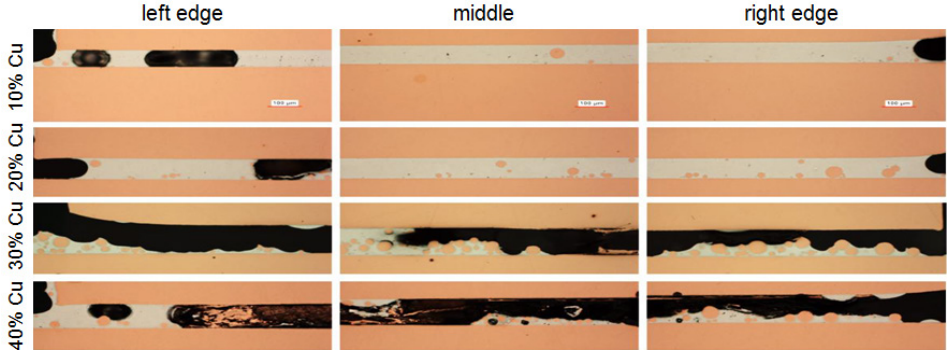


Figure 114: Pore formation by increasing of copper mass-fraction in the composite solder approach [67; 130].

The influence of the copper content can be explained with the investigations in CAPM technology for the treatment of solder pastes for accelerated IMP formation. As introduced in the sub-chapter 5.2, the printed solder layers were treated with copper particles to increase the copper fraction in solder layer and procure copper for diffusion from the chip backside. The resultant height of the coated interlayer was dependent on the number of runs on the printed solder layer. It was observed that the Cu-coating with

plasma activation had significant influence on the copper filling. The assemblies from Figure 115 were soldered with VVP soldering with peak time of 15 min at 260 °C. These show firstly, a bondline thickness up to 80 µm with partial transformation showing clusters of IMPs of Cu_6Sn_5 in the whole bondline. This also confirms that introduction of copper through CAPM is as alternative to composite solder paste or lateral flow TLPS approaches. Figure 116 shows the CAPM enhanced thicker TLPS joints of 50 µm and 80 µm thicknesses with full IMP transformation in the bondline. In both the figures, rest tin clusters in both the pictures are visible. Figure 117c shows a fully transformed with no rest tin or voids.

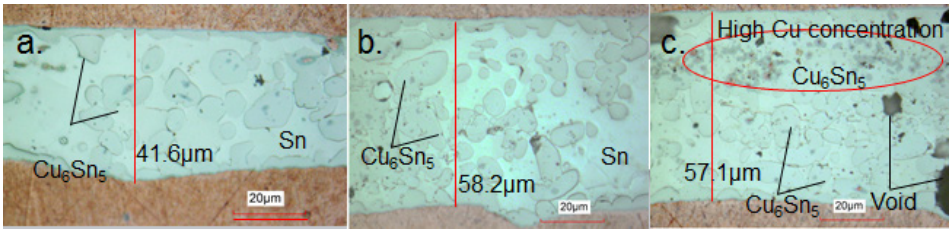


Figure 115: Influence of CAPM coated Cu-particles in the interlayer for local IMP formation in addition to the IMP formation at the interfaces; a,b. type 6; c.type 7.

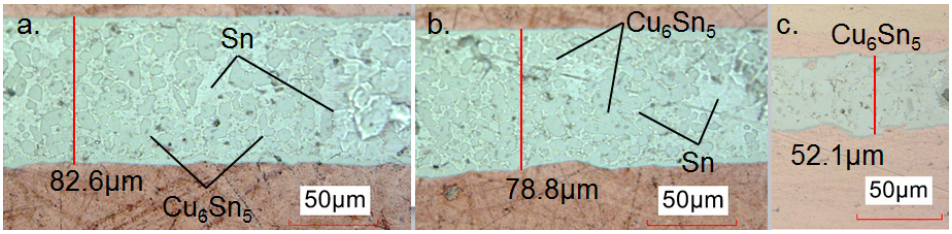


Figure 116: Produced CAPM-enhanced TLPS interconnects up to 80 µm thickness with Cu_6Sn_5 islands over the complete bondline.

Solder paste type

The test assemblies were prepared with 110 µm stencil printing with solder pastes of types 6 and type 7. Generally, for better solder paste printability and shelf life, type 7 has high fluidic solvent material. It can be seen from Figure 118, that the type 6 paste had a better phase growth. This effect can be explained homogenous distribution of Sn and Cu particles in the solder deposit and deeper penetration of sprayed copper particles into the solder depot through the matrix. Due to high fluidic content in type 7, the copper particles had shown high affinity to adhere to top layers without penetration as in Figure 115c.

CAPM coating methodology

The IMP formations as shown in Figure 118 with plasma assisted copper coating (Strategy S1) were significantly better compared to copper coating without plasma activation (Strategy S2). As the print pressure with plasma activation is significantly higher during the powder deposition, the copper particles penetrate deeper into the solder deposit and therefore are distributed homogenously in the solder depot. The initial IMP formation during the thermal treatment starts from the bottom of the solder layer on topside copper of DCB substrate, creating favorable starting conditions for IMP cluster formation from the coated copper particles. The strategy S1 evidently produced higher IMPs >20 µm compared to the strategy S2 <20 µm without plasma activation.

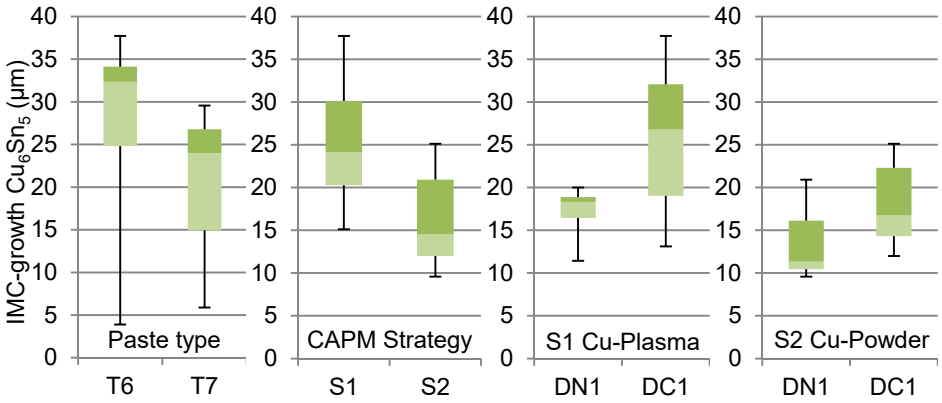


Figure 117: (left to right) Dependence of IMP formation for the used solder paste type (type 6 and type 7); CAPM strategies S1 and S2; for 6.25mm² components with nickel (DN1) and copper metallization (DC1) for S1 and S2.

Component metallization

The above figure also shows the comparative growth of Cu_6Sn_5 phase for Ni-Ag metallized semiconductor chips (DN1) and the Cu-metallized dummy components (DC1) with different application methodologies S1 and S2 as introduced in sub-chapter 5.2. In both S1 and S2, it can be clearly seen that additional copper on the component surface led to better growth phase in the solder joint. From the copper coating, additional copper diffuses into the tin of solder which directly affect the diffusion paths for IMP formation at copper particles from CAPM process. Since the diffusion paths are mainly in the direction of decreasing copper concentration, the additionally introduced copper particles enhances the IMP growth processes in the center of the solder layer.

Thermal treatment

The reaction kinetics of the IMP formation depended mainly on the temperature treatment together with the material composition in the interlayer. The heat transfer by convection and condensation were tested to analyze the IMP growth. The condensation (vapor phase) soldering ensured a consistent and homogenous heat input and a better IMP formation compared to convection resulting in near to 30 µm of η-IMPs in the interlayers in 18 min as in Figure 118. Without copper particles on solder depots, a temperature treatment of 55 min at 250 °C was needed, which was greatly reduced to <20 min with CAPM treated solder layers. Based upon previous energy consumption investigations of complete process chain from paste printing to soldering, it was inferred that a 30% savings potential is possible with plasma enhanced TLPS compared to state-of-the-art TLPS methodologies.

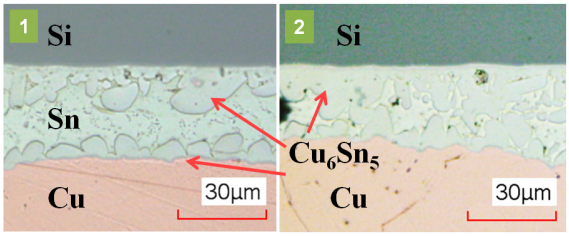


Figure 118: Cross sections for the produced TLPS diffusion soldered joints with two different heat-transfer mechanisms: 1. OPC and 2. VVP.

7.3 Characterization of Produced TLPS Interconnects

After a successful selection of the profile parameters and production of the TLPS interconnections, the assemblies were analyzed for the IMP formation and the process-, material- related defects. The joint quality is accessed by means of shear tests at room and high temperatures.

7.3.1 Defect Analysis

As explained in the sub-chapter 2.4 on the voiding characteristics in conventional solder joints, the dominating voids are generally interfacial macro-voids or shrinkage voids due to residual gases. From literature, in case of diffusion soldering with full ε-Cu_3Sn IMP, there are mainly two types of defects as shown in Figure 119. These are termed as bond-interface voids at the middle of the bondline and Kirkendall voids at Cu/Cu_3Sn interfaces. The bond interface voids are formed due to consumption of Cu_6Sn_5 IMPs

in Cu_3Sn formation. These could have formed also due to deficit tin initially during Cu_6Sn_5 formation. The Kirkendall voids are due to the copper atom diffusion into Cu_6Sn_5 IMP from the already formed Cu_3Sn phases at the interfaces. This is hugely influenced by the applied mechanical pressure during bonding process, where copper atoms are not forcibly diffused leading to nano-voids.

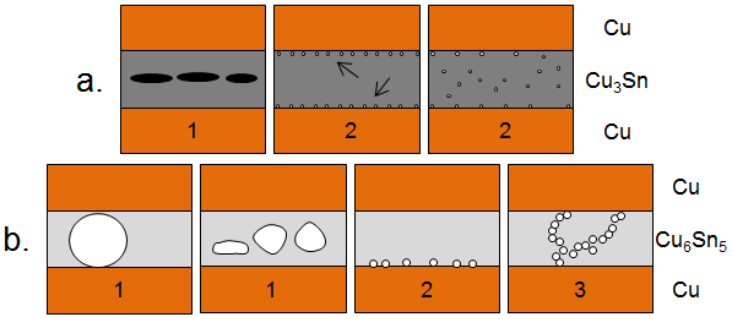


Figure 119: Types of defects/ voids observed in a. TLPB technique with Cu_3Sn bondline [188; 189]; b. TLPS with Cu_6Sn_5 bondline from the present work.

As the main focus in this work was to optimize the production methodology to be able to produce TLPS with conventional production equipment, the process is stopped only till the Cu_6Sn_5 are formed. These above explained voids especially Figure 119.a. do not occur in case of bondlines with Cu_6Sn_5 IMPs. As the followed TLPS approaches are low-pressure or pressure less interconnection processes, a different set of defects were observed as shown in Figure 119b in this work:

- voids due to flux material residues in the bondline (b1)
- the bond-interface voids due to tin deficit during IMP formation (b1)
- nano-voids at boundaries during the IMP grain growth and coarsening (b2)
- skeleton formation in case of CAPM TLPS methodology (b3)

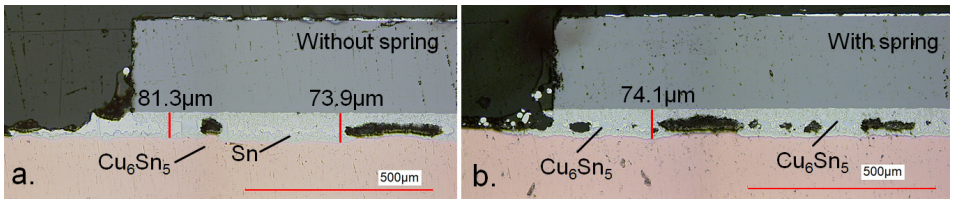


Figure 120: Influence of spring support in the IMP formation with increased voids.

In Figure 120, the influence of the assemblies with and without spring structures during TLPS is shown. Here the influence of low pressure can be observed, where the IMP formation increased significantly compared to

assembly without spring support. It can be observed that the defects were comparatively higher in the bondline dominated by the bond interface voids due to rougher surfaces and deficit of tin material in the interlayer. In Figure 121 of TLPS approach A1, it can be seen that the roughness has significant influence in the realization of full IMP formation. The effect of the paste type is also seen depending on the roughness of the substrate. The type 7 paste materials had overall better quality of IMPs compared to type 6 or type 8. For type 6 particle size, the critical interlayer thickness did not comply leading to initial void formation and unwetted areas.

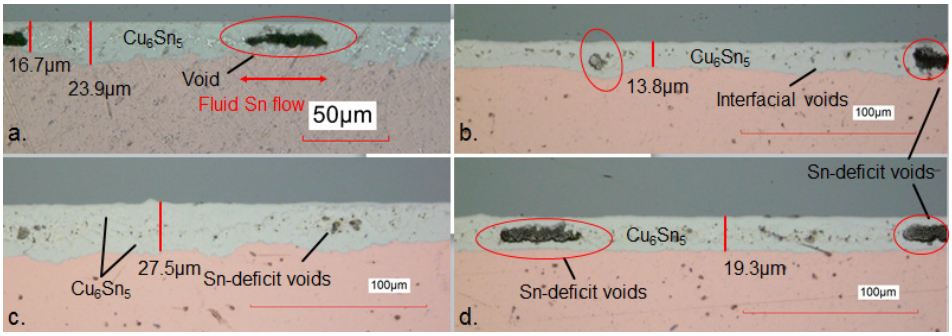


Figure 121: Defects observed in the paste-based TLPS approach A1 for the solder pastes of a. type 6, b,c. type 7, d. type 8.

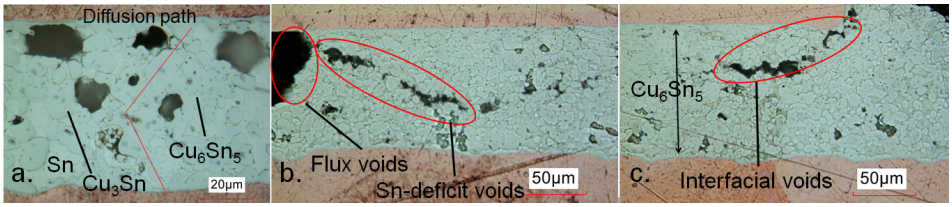


Figure 122: Types of voids observed in the CAPM enhanced TLPS.

The Figure 122 shows the defects in case of approach A2 of CAPM enhanced TLPS. These were generally the tin deficit voids (a,b) as in approach A1 and also micro-voids and boundary interface voids (b,c) at the grains of individual IMP clusters.

7.3.2 Comparison of the Joint Quality

The comparison of the TLPS joint quality was performed by destructive shear tests at various temperatures. To obtain comparable results with the tested TLPS variants with solder pastes and preforms, the component sizes of 25 mm² with standard Ni-Ag and Cu metallization were considered. It was made sure that the samples were thermal treated for a full IMP growth

in the bondline with low defects. In case of paste based TLPS, voids due to flux materials and improper outgassing could not be avoided. The fracture modes obtained for room-temperature shear tests in case of paste-based and preform-based TLPS are shown in Figure 123. The component metallization and the void areas were observed as the weak spots compared to the interconnection itself. For the preform-based TLPS, only the component fractures were observed due to the brittle nature of the silicon semiconductor materials.

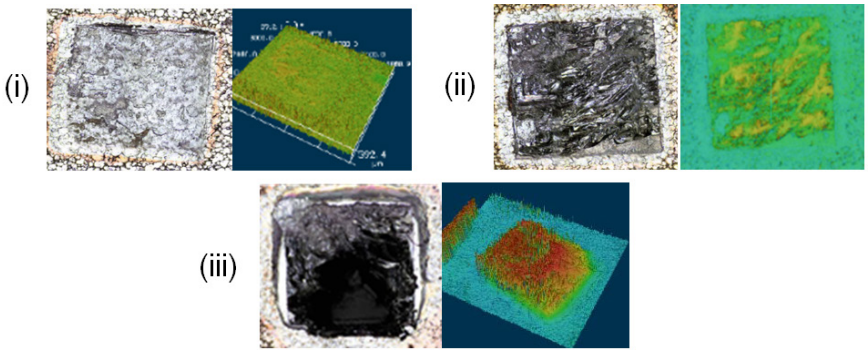


Figure 123: Fracture modes observed in the shear tests (i) metallization fracture, (ii) mixed fracture, (iii) component fracture.

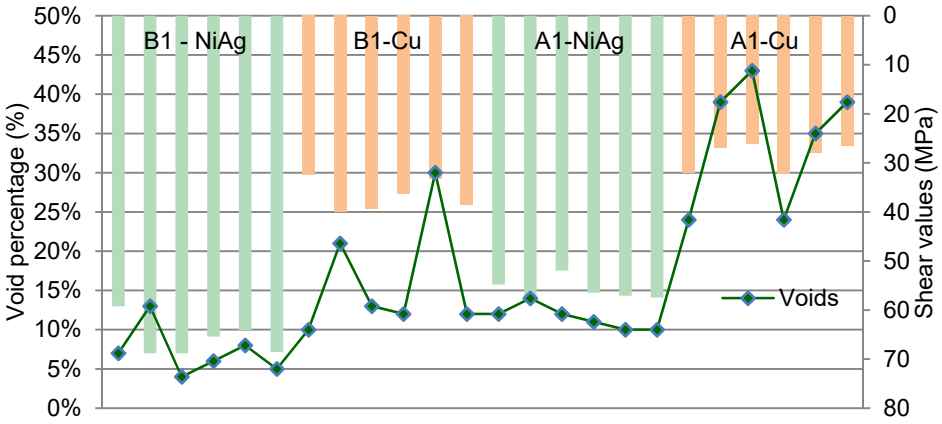


Figure 124: Overview of the shear values with void percentages for approaches A1 (paste based) and B1 (preform based) with components of varying chip back-side metallization.

The Figure 124 gives an overview of the dependence of shear values with respect to void percentages for the standard NiAg and Cu component metallizations. The Cu metallized components in approach A1 had relatively high void percentages > 30% with shear values between 20 – 30 MPa. For NiAg chips, the shear code was always the metallization fracture and

for Cu-chips, mixed fracture of component and IMP bondline. However in case of approach B1, the shear code was at the interface with shear values up to 70 MPa for void percentages ~5%. For Cu-chips, though the wetting was very good, the shear code of always the component break wuith shear values between 30 - 40 MPa.

The dependence of shear values with high temperature is shown in Figure 125 through the loss of adhesion tests up to 450 °C for the TLPS assemblies. The figure shows that the produced TLPS joints had a high and stable adhesion up to 350 °C and declined gradually up to 425 °C. This proves that the selected thermal treatment profiles produce IMPs in the complete bondline compared to loss of adhesion in interconnects with tin materials in case of standard solder joints.

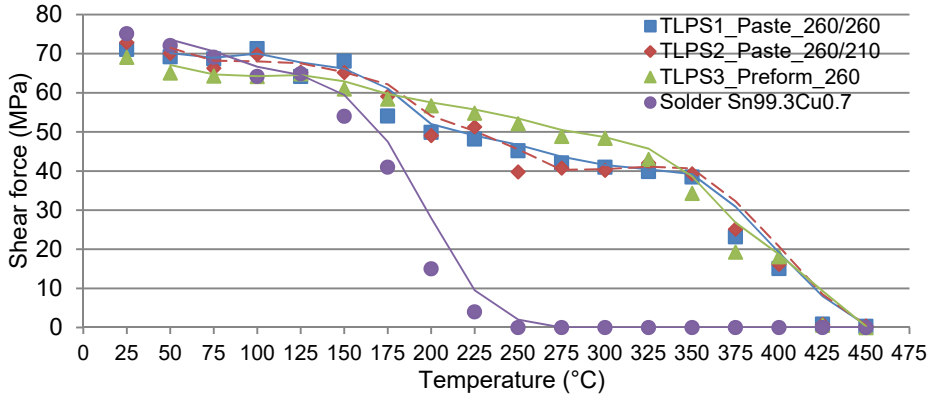


Figure 125: Loss of adhesion tests upto 450 °C performed for conventional solder $Sn_{99.3}Cu_{0.7}$, paste- and preform-based TLPS interconnections.

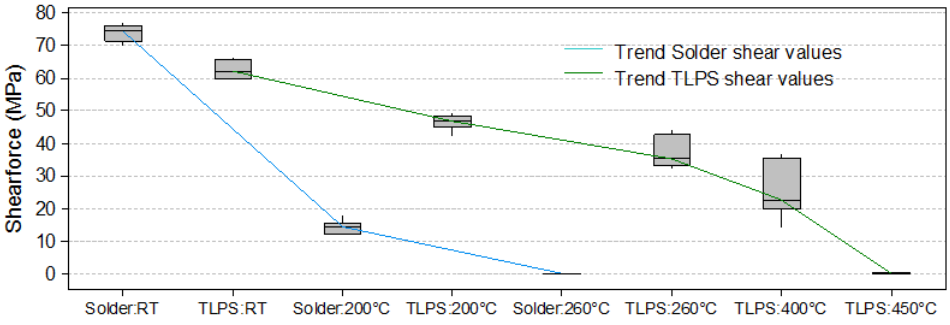


Figure 126: Overview of the shear values obtained at various temperatures for the conventional solder with $Sn_{99.3}Cu_{0.7}$ and Sn-Cu paste-based TLPS interconnects.

Figure 127 also shows the performed high-temperature shear tests up to 450 °C. The comparison of the shear values show that the TLPS approach followed had good high temperature stability upto the melting points of Cu_6Sn_5 i.e. 416 °C. For the higher temperature shear tests, as explained above in the fracture modes, majority of the shear codes were observed at the metallization interface between the chip and IMP bondline. The variation in the shear tests can be attributed to the quality of the TLPS interconnects. At higher temperatures 260 °C and 400 °C i.e. greater than melting point of tin, the interconnects displayed stable shear values above 20 MPa.

7.4 Temperature Cycling Tests

The accelerated reliability tests were performed for the assemblies with paste based and preform based TLPS interconnects. Temperature shock tests of -40 °C/+125 °C and -40°C/+150 °C were performed to check the degradation and crack formations. The assemblies from the investigated approaches of preform-based TLPS (B1), paste-based TLPS (A1) and CAPM-enhanced TLPS (A2) were used in the temperature cycling tests. A total of 1100 cycles of -40 °C/+150 °C were performed and used further in defect analysis. As shown in Figure 127, the preform based interconnects showed comparatively good performance up to 1000 cycles with stable shear strengths above 40 MPa. However the paste-based TLPS had a decreasing trend for mechanical stability after 500 cycles due to the voids. This was due to the degradation of the rest tin material and crack formation and propagation. Due to lower void percentages and full transformation into IMPs in case of preform-based TLPS, no specific cracks were observed till 750 cycles.

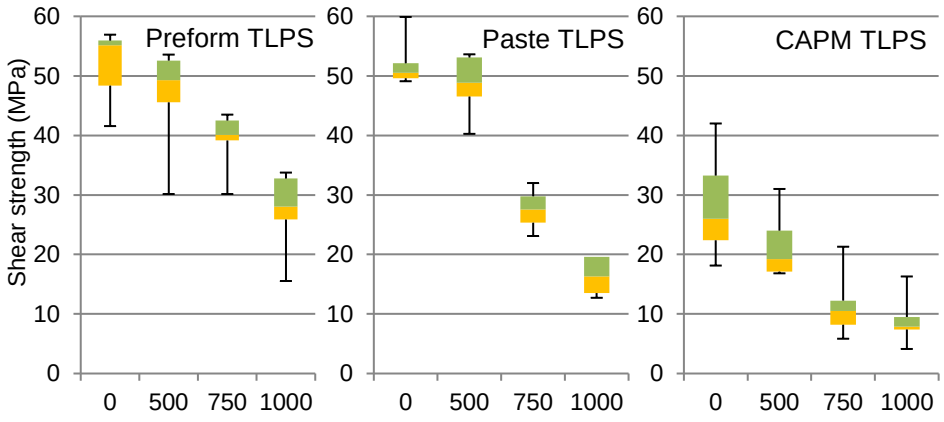


Figure 127: Overview of the shear values for the temperature cycling tests of -40 °C/+150 °C for the investigated TLPS approaches.

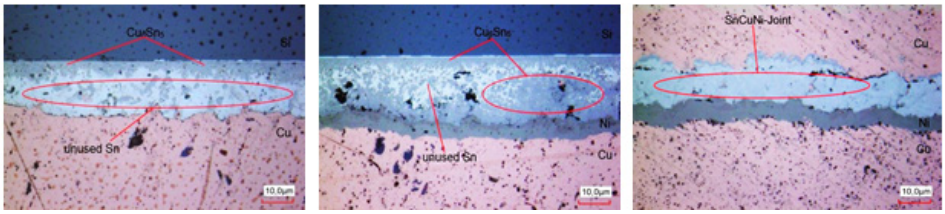


Figure 128: Cross-section images of the temperature cycles samples at -40 °C/+125°C after 500 cycles [186].

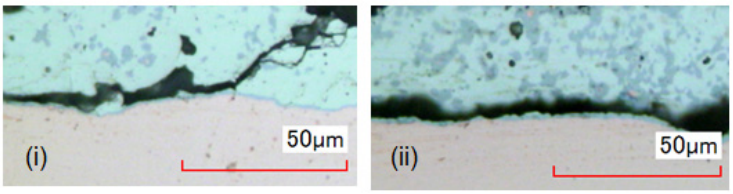


Figure 129: Delamination at Cu_3Sn IMP/ Cu DCB interface in test samples with (i) Silicon chip and (ii) dummy component observed after 2250 temperature cycles of -40 °C/+125°C [147].

Temperature shock tests (-40 °C/+125 °C) were run up to 2500 cycles with cycle time of 15 min to check the joint stability and adhesion characteristics. Both paste- and preform-based TLPS was stable without any visible defects of delaminations or crack propagations. As it seen in Figure 129 of cross sections, the cracks were observed at the interface between Cu/Cu_6Sn_5 at Cu_3Sn IMPs. It can also be observed that the interfaces between Cu_6Sn_5 grains were transformed into Cu_3Sn phases. The crack propagation was observed from the formed kirkendall voids to the voids in the IMP bondline.

The Figure 130 shows also the shear codes after 1200 cycles of TLPS interconnects of approachs A1a Cu- metallized dummy component and A1b for standard NiAg metallized silicon chip. The chip backside images (i,iii) show the mixed fracture code after the shear tests with shear values of approx. 50 MPa.

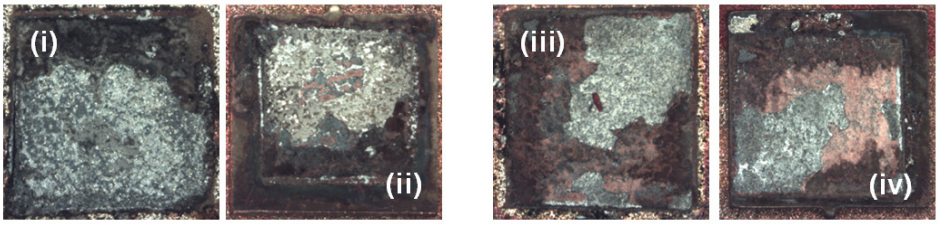


Figure 130: Delamination at Cu_3Sn IMP/ Cu DCB interface in test samples with (i,ii) Silicon chip and (iii,iv) dummy component observed in shear tests after 1200 temperature cycles [147].

The test assemblies of the paste-based TLPS were also stored at high temperatures to observe the IMP formation. The bondline was fully transformed into IMPs even in case of Ni-DCB substrates. However in this case an increased Cu_3Sn phase was observed indicating the formation of micro-voids at the joint interface.

8 Adaptability and Concepts for TLPS Production

8.1 Demonstrations of the Diffusion Soldering Technology

The developed test profiles introduced in section 7.1.2 were selected and used for the demonstration of TLPS as a die-attach technology. The aim of these demonstrations was to check the compatibility and reproducibility of the developed TLPS approaches for serial production. The automation potential for two product series was checked for customization and integration flexibility followed by the quality control and testing. The objective of the technology study was to check the feasibility of producing TLPB joints with the developed TLPS profiles and fixtures for the bonding process. The influence of the CFL soldering i.e. forming gas and formic acid handling on TLPB samples was also observed and analyzed for defects [190].

8.1.1 Product Study: Production of TLPS based Multi-chip Packages

The scientific objective was to check the reproducibility of the assemblies with TLPS technology with various preforms, substrate metallizations and product designs. The production of the assemblies was performed at the production equipment of Powersem GmbH, Germany to check compatibility of the developed TLPS approach for serial production. The process flow is shown in Figure 131 where the preforms and components were placed into soldering jigs as explained in section 7.1.3. This was followed by the TLPS with the selection of preforms according to the substrate metallization. The developed preforms of various thicknesses were used as interlayer materials to investigate the errors during placement.

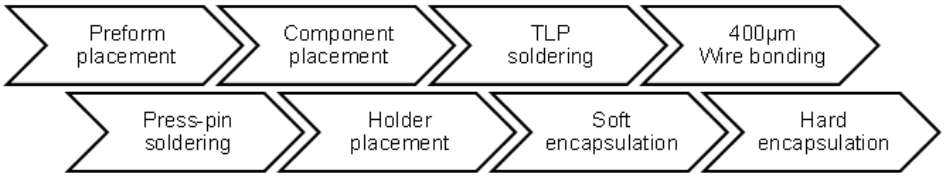


Figure 131: Process flow for the production of TLPS based press-pin packages.

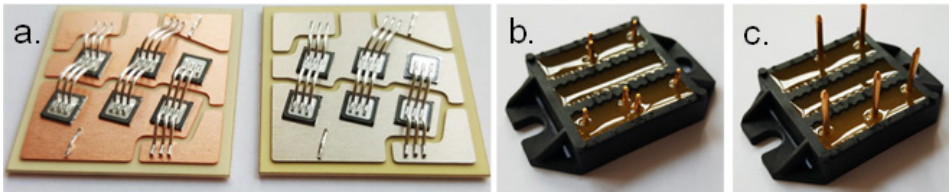


Figure 132: Technology demonstrators showing the multi-chip press-pin packages: a. TLPS and 400 µm wire bonding on Cu-DCB (left) and Ni-DCB (right); b, c. Press-pin based packages with TLPS as die-attach.

After the preform-based TLPS, the modules were heavy wire bonded with 400 µm diameter wires as shown in Figure 132. The press-pin were selected according to the product layout and soft soldered onto the wire-bonded DCBs followed by the encapsulation of the components as shown in Figure 132.b.c. For the production of these modules, a high product customization was possible due to flexible material selection and placement. The TLP soldering was performed for approximately 50 modules per batch in the CFL inline soldering system.

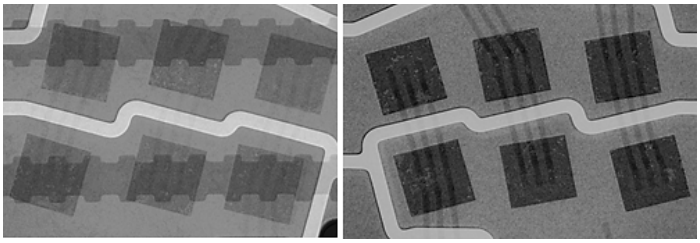


Figure 133: X-ray images of the TLPS based multi-chip packages: Cu-DCB based press-pin package with B1P1 preforms (left) and B2PC preforms (right).

The produced test assemblies were further analyzed for defects and quality control with reverse bias and voltage drop tests. It can be observed from the X-ray images from Figure 133 that the obtained power modules had evidently less than 3% voids for each component. A high customization of the TLPS technique was possible for serial production irrespective of the type of materials or product designs used. The TLPS technique would eventually be investigated in future for other modules and scalability for serial production in other production facilities of Powersem GmbH.

8.1.2 Technology Study: Production of TLPB Interconnects

As a technology study, the developed TLPS approach was applied to TLPB of Cu-Sn and Ag-Sn bimetallic systems to observe the bonding characteristics and defects. For this, copper bars of thickness 3 mm with corresponding metallizations were bonded with each other. The bars were bonded in the

CFL soldering machines with formic acid handling and forming gas as process gas similar to preform based fluxless TLPS as in above sub-chapter 8.1.1. The materials were provided by the School of Engineering, University of Warwick, United Kingdom.

The copper bars of were prepared from 10 cm x 10 cm copper plates which were initially fine polished and nickel-phosphorus (Ni-P) electroless plated to 5 - 6 µm thickness. As metallization for the above bimetallic combinations, the copper plates were over-plated with electroless copper of approx. 5 µm and a final plating of electroplated tin of approx. 10 µm for Cu-Sn TLP joints. For Ag-Sn TLP joints, the surfaces were electroless plated with silver and then tin on Ni-P layers. A few aluminum silicon carbide (AlSiC) plates were also plated with silver followed by tin. These metallized copper plated were cut into 9 mm x 5 mm for the bonding tests. The layer structures can be seen in Figure 135 and Figure 137. For the bonding experiments, the test bars as shown in Figure 134 were fixed together in pairs according to combination in a specially-prepared sample holder with screw clamps. The bonding process with the developed TLPS profile resulted in good bondline with low or no voids. The corresponding bondlines and observed defects are summarized in following sections.

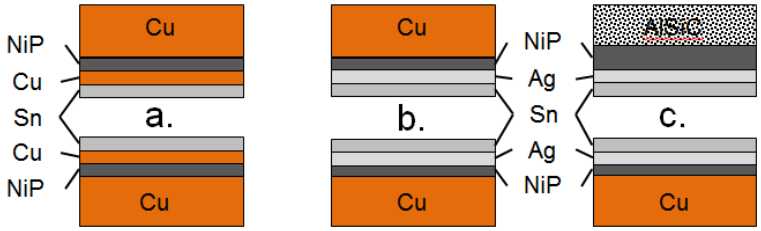


Figure 134: Sketch of the supplied materials according to the approach Cu-Sn TLPB with a. Cu-Cu bar; Ag-Sn TLPB with b. Cu-Cu; c. Cu-AlSiC bars.

Cu-Sn TLPB demonstration:

In case of the Cu-Sn TLPB tests, an excellent bondline was obtained with fully transformed η-IMP. It can be observed from the Figure 136 that with 10 µm Sn and 5 µm on each bar, the phase formation was complete with bondline thickness of approx. 10 µm. Few regions of unused tin were also observed for bondlines of thickness > 12 µm. Depending on the surface profile of the electroless copper layers, the Cu_3Sn IMP topology can be observed with thickness of 1 - 2 µm.

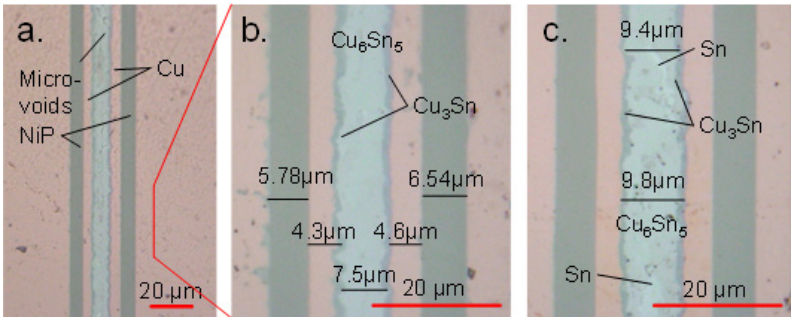


Figure 135: Cross-sectional images of the obtained Cu-Sn TLPB joint with bondlines between 7 to 10 µm fully transformed η-Cu_6Sn_5 IMP.

The FIB images in Figure 136 show the defect regions of the interfacial voids. It can be interpreted that though no void structures were observed in cross-sections, lateral interfacial voids up to 30 µm were observed. The tin in this case was completed used and the topology of the already formed IMPs in the bondlines can be seen. The IMP boundary grains can be seen clearly in Figure 136.b indicating the deficit of interlayer material. An increased fixture pressure or increased tin layer up to 15 µm would reduce the voiding in the bondlines.

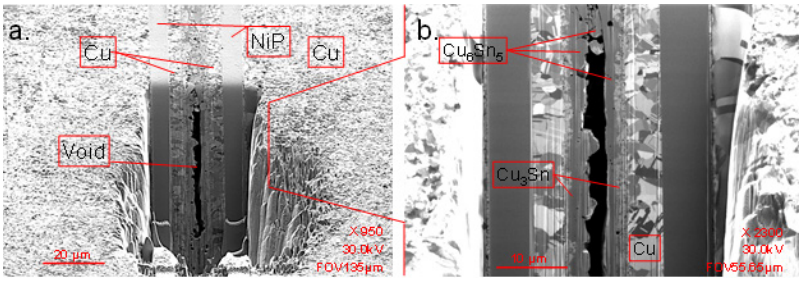


Figure 136: FIB images of the Cu-Sn interconnect showing the interfacial voids due to the deficit of interlayer tin material.

Ag-Sn TLPB demonstration:

Similarly Cu/AlSiC and Cu/Cu paired bars were bonded with the plated Ag and Sn layers. Here the bonding temperature was set to 280 °C compared to 260 °C in case of Cu-Sn based TLPB joints. It can be observed from the Figure 137 that the bondlines were fully transformed into Ag_3Sn layers. It can be observed that the Ni-P layers on AlSiC side are thicker compared to Cu side, this is to make the AlSiC surface uniform for high quality TLPB. In case of CTE mismatched pairs i.e Cu/ AlSiC, the uneven expansion let to the formation of lateral interfacial voids in few cases as shown in Figure

139.b. The FIB images as in Figure 138 show that even a complete IMP formation was possible, lateral voids were found showing the grain topology. The silver material can be also observed in the bondline next to the Ni-P passivation layers.

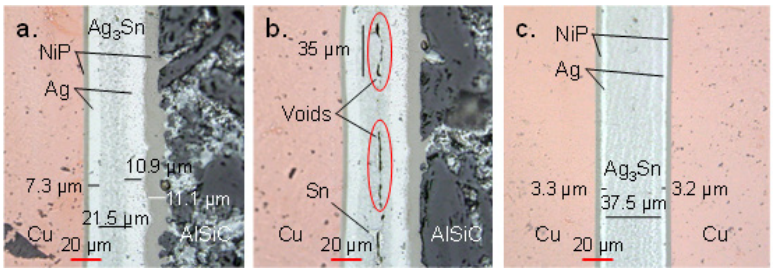


Figure 137: Cross-sectional images of the obtained Ag-Sn TLPB joint with 37 µm full transformed Ag_3Sn IMP.

Figure 139.a,b shows the interfacial voids and grain boundaries in the bondlines. The size of the formed voids can be explained by the neighboring IMP grain size. It can also be observed in Figure 139.c,d, that the nanovoids between the individual grains had size from 300 nm to 1 µm.

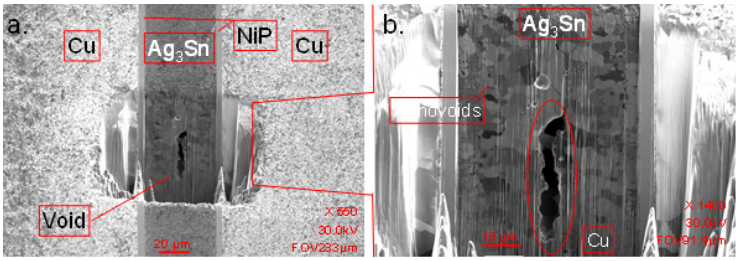


Figure 138: FIB images of the Ag-Sn interconnect showing the interfacial voids due to the deficit of interlayer tin material.

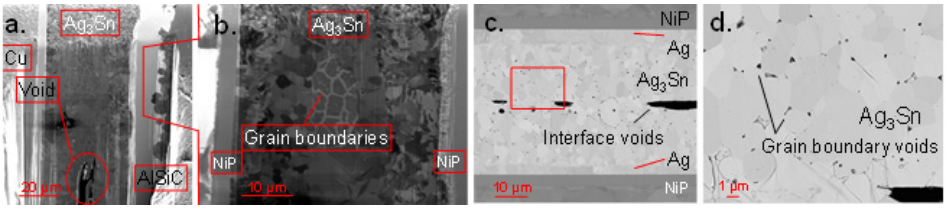


Figure 139: FIB and microscopic images of the Ag-Sn interconnect showing the interfacial and grain boundary micro-voids.

From this technology study, it can be inferred that the developed TLPS profiles can also be used for the TLPB of various systems with slight modification of the peak temperatures. A higher quality of the TLP joints was obtained compared to the traditional vacuum bonding processes. This can

be attributed to the initial formic acid handling for removal of the oxides and impurities from the copper surfaces. The clamped bonding support for the samples provided the required supporting bonding force to keep the material generated defects to minimum.

8.2 Comparison and Flexibility of the TLPS Approaches

The selection of the key profile parameters according to the machine are interlinked also with the materials used for the TLPS process. The production lines for the followed approaches are outlined in the Figure 140. It can be clearly observed that the preform-based CFL soldering has the low overall process time compared to the other approaches in achieving fully transformed TLPS.

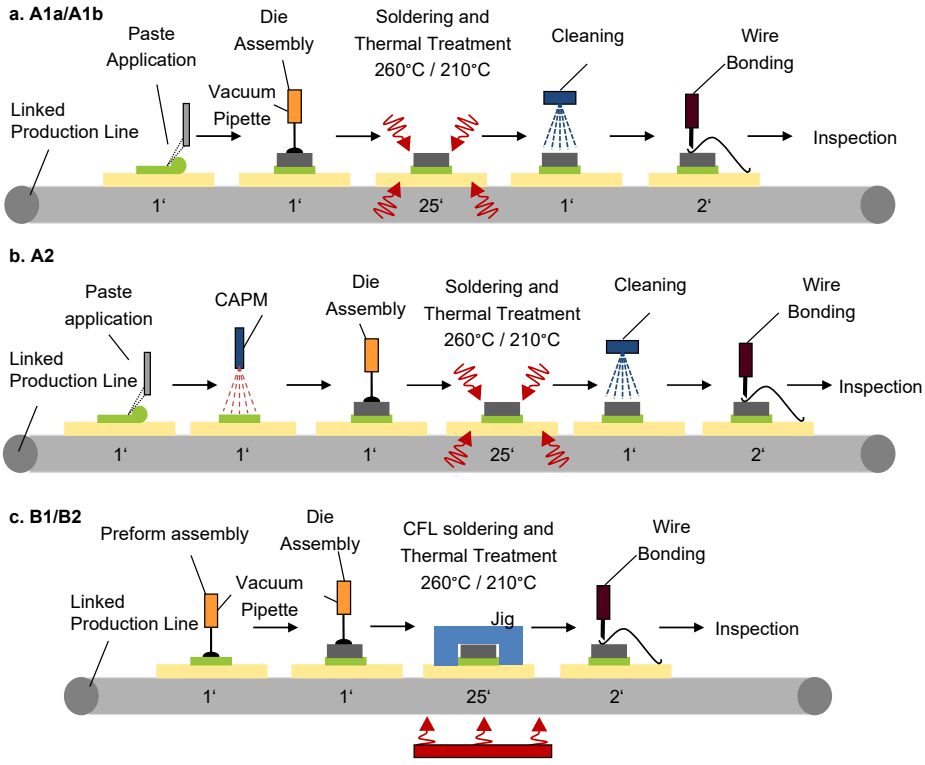


Figure 140: Schematic comparison of the followed approaches a. Paste based TLPS; b. CAPM enhanced TLPS; c. Preform-based TLPS.

The paste-based TLPS is the nearest to the conventional production techniques which can be implemented without any equipment modification.

But here a high quality of the TLPS requires control of the process influential factors and depends on the material selection mainly the solder paste type and substrate. However for TLPS with thicker bondlines, the integration of CAPM technique for the introduction of copper particles in solder layers effectively enhances the bondlines with connected IMPs. This technique also procures enough copper particles on the solder depot along with increasing the copper content in the interlayer material to realize TLPS more effectively.

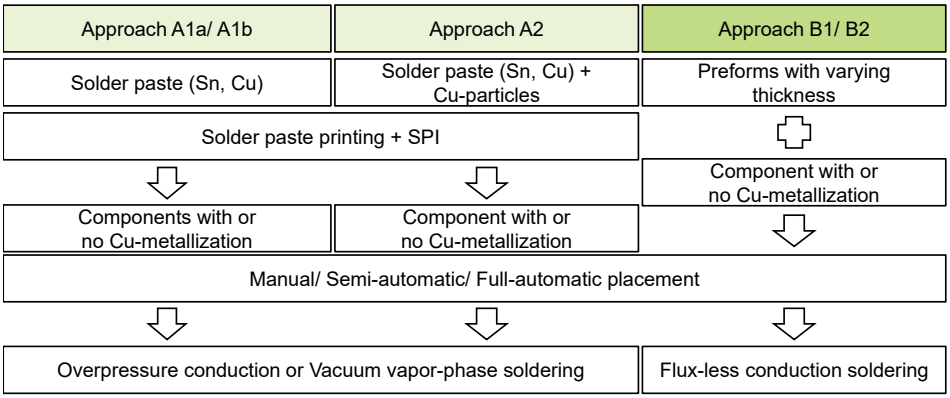


Figure 141: Comparison of the followed TLPS approaches with customizability of usable material and components.

In the approaches with solder paste interlayers or thermal treatment, additional cleaning steps are required to obtain high quality surfaces for wire bonding. In case of fluxless preforms, the thermally treated assemblies were ready for wire bonding without requiring any cleaning or inspection increasing significantly the production throughput.

8.3 Conclusion and Outlook for Diffusion Soldering

This sub-chapter gives the conclusions from investigations detailed in the chapter 7 and sub-chapter 8.1 followed by the outlook for machine concepts and material systems. In the perspective of the industry requirements on reliable and economical production of power assemblies with high temperature capability, the TLPS technique is the nearest to the conventional technologies with the potential of high flexibility and customization. This enables the use of the already available soldering equipment in the power electronics production with slight modifications of materials and profile concepts. From the Table 31, it can be observed that the obtained IMPs and process complexities are comparatively simpler compared to silver sintering or TLPB techniques.

Table 31: Comparison of the die-attach technologies with respect to complexity.

Process	Melting temperature (T_m) of the interlayer	Process temperature	Material costs	Complexity of the process
Soldering	231.9 °C (Sn)	Low	Low	Low
Sintering	961.7 °C (Ag)	Medium	Very high	High (pressure assisted)
TLPB	415 °C (Cu_6Sn_5), 676 °C (Cu_3Sn)	Low/ Medium	Medium	High (pressure assisted)
TLPS	415 °C (Cu_6Sn_5), 676 °C (Cu_3Sn)	Low/ Medium	Low	No to low

8.3.1 Machine concept

The investigations with various component dimensions in the TLPS technique showed that for smaller components less than 30 mm² either with or without copper metallization, the energy transfer was adequate for full IMP transformation without any mechanical pressure. In case of semiconductor chips with Cu- frontside metallization, a supporting pressure was required to ensure low warpage and full IMP growth. In case of CFL soldering, the assemblies were supported by the graphite jigs for the homogenous energy transfer, positioning and for the spring supports on top of the semiconductor components. The pressure variation with combination of multiple vacuum and overpressure indicated excellent void content with negligible defects and full IMP growth in the bondline with various flux-less preforms. As introduced in chapter 6.3 and section 7.1.2, a combination of vacuum and overpressure highly enhanced the quality of the TLPS joints.

Even in case paste-based TLPS with OPC and VVP soldering, low-void bondlines are obtained with post thermal treatment less than melting points of tin i.e. 210 °C. The overpressure in the hyper pneumatic chamber supported the void reduction and partially the IMP growth. However, in case of VVP technique, though the IMP growth was comparatively slower, but was compensated by the high energy transfer from the galden medium at 260 °C. Further machine related concepts however should focus just not on treating the assemblies thermally, but include concepts for faster IMP transformation by combining the advantages of interlayer material modifications and machine related optimization. For the OPC soldering machine, as described in section 6.3.2 on the pressure variation with combination of vacuum and overpressure, a hardware modification to equip vacuum in the same hyper pneumatic chamber could significantly reduce the voids

formed during the flux activation and outgassing. A supportive post-handling treatment following the main temperature and pressure profile at atmospheric pressure or overpressure ensures full IMP formation in the bondline. For this, a lateral post-thermal i.e. paternoster machine concept with assemblies running in vertical direction (First-in/ First-out) can be a realizable idea to save space in perspective of serial or mass production of TLPS interconnections.

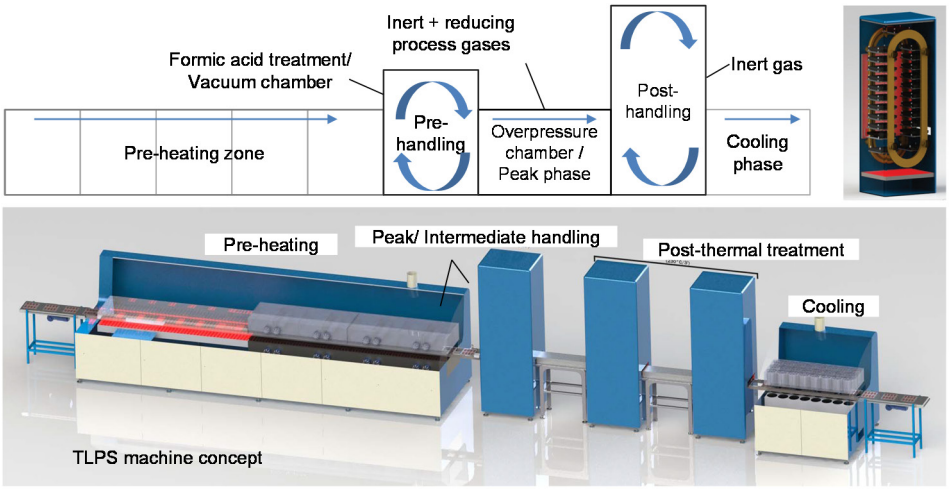


Figure 142: Machine concept for TLPS process with modular modification with pre- and post-handling chamber.

Figure 142 shows the machine concepts for intended prolonged thermal treatment. The CAD models have been provided by the Seho systems on behalf of the cooperative work performed during the ProPower project. The paternoster systems can be installed flexibly according to the profile. This machine concept can be easily modified for the sintering technologies with custom made work piece carriers. This avoids the investments regarding complex hydraulic pressure units. A work piece carrier model is given in Figure 143.

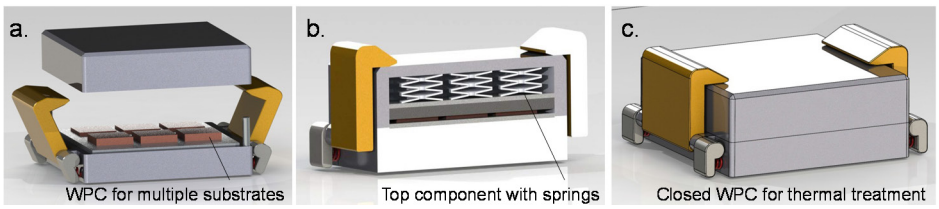


Figure 143: Multi-purpose work piece carrier model for TLPS process.

The WPC model has numerous advantages concerning the flexibility of the power modules. Here the spring support can be designed individually according to the circuit or component layout. This also supports pressure alignment for designs with varying component heights and also parallelly avoids warpage of the components. The spring system can also be replaced with CTE controlled pressure mechanism.

For the VVP soldering, a combination of vacuum profile with low-pressure assistance mechanically and locally on the chip can accelerate the IMP formation keeping the void percentage to minimum. A modification of VVP soldering with overpressure produced through the condensation medium could be an interesting approach with applications in rework of conventional electronic assemblies. But this is linked with machine related complications in generating controlled spray of high-temperature galden.

Table 32: TLPS variants and possible machine concepts for production

TLPS machine variants	Description/ suggestion	Pros & Cons
Pressure-less thermal treatment	Vertical paternoster system for post-thermal treatment at temperatures below melting point (with individual multi-substrate carriers) after initial solder profile	Longer process time
Overpressure-assisted	Multiple pressure cycles in combination with vacuum	Intermediate process time and high quality
Pressure-assisted (high)	Assisted by modular CTE controlled pressure mechanism on WPC with uniform pressure as in silver sintering at the peak temperatures	Equipment investment
Pressure-assisted (low)	Assisted by mech. Jigs and spring structures in WPC and thermal treatment with conventional soldering machines	Intermediate process time and high quality

8.3.2 Interlayer Material Solutions

The TLPS process has been successfully investigated and demonstrated by used Cu-Sn based soft solders and preforms materials. Based on the analysis, for a reliable and fully transformed bondlines, adequate copper must be made available. This becomes crucial if thicker bondlines with fully transformed IMPs are to be achieved. In this thesis, this was demonstrated by using CAPM technology on solder depots in case of paste based TLPS and through multi-layer preforms in case of preform based TLPS. Depending on the amount of tin (average of 10 µm) to be transformed, a profile time of 25 min at 260 °C was required. This was also possible by standard reflow followed by post thermal treatment with low-pressure support at 210 °C with total handling time of 35 min.

As further material solutions for the paste based TLPS, similar to composite solder pastes, the pastes can be formulated with other additives like Ni for Ni-plated substrates and low melting elements like bismuth or indium. Further additions for lead-free alternative can be ferro- or paramagnetic particles dispersed in the alloy. This enables remote control and manipulation of composite alloy with magnetic fields and parallelly enhancing the mechanical properties [191]. Such particles can also be used in procuring additional energy to accelerate the IMP transformation by manipulating the magnetic fields. A further outlook can be additions of particles with CTE between silicon and copper to enhance the reliability performance [192]. This technique is newly introduced in the silver sintering materials to reduce the porosities with particles like wolfram, molybdenum or Ag coated Ni particles. This enables also the reduction of processing temperatures of the sintering materials to obtain good quality of bondlines. A similar combination of materials can also significantly reduce the processing temperature or enhance the IMP formation at intermediate temperatures in less time.

The process and the influential parameters for the development of preform based TLPS has been evaluated and summarized. The process had been modified for high flexibility and customization of products. Particularly in Cu-Sn based preforms, the wetting characteristics and voiding was excellent on bare DCB substrates with fully transformed η IMPs in the bondline. The Cu-Sn-Ni suits preferably better for Ni-plated DCB substrates, however improper wetting characteristics led to void structures in bondline which evidently led to incomplete IMP transformation for same temperature profiles. The cladded preforms B2PC showed excellent wetting and η phases with void-free bondline. The usage of Sn-Cu-Sn cladded version improved

the handling of preforms during assembly and the TLPS process as well. It can be inferred that the copper from the preform was used in the accelerated development of IMP from middle of the bond-line resulting in full transformation into η-phases in shorter time compared to thin preforms irrespective of the component metallizations.

For the preform based TLPS, the uniformity and thickness of the preform highly influences the complete transformation into IMPs. The bondline thickness (after soldering < 15 µm) is suggested for the intended diffusion length. The preforms require appropriate handling and precise positioning during the assembly process. An offset in the positioning might result in improper wetting and incomplete IMP transformation. For this purpose, a thicker preform can be developed accordingly, but with smaller dimensions to obtain appropriate bondline of less than 15 µm during the soldering process.

For cladded preform designs, a minimum of 40 µm copper layer with ~20 µm of Sn on both sides adding to a total preform thickness of 80 µm, enables full IMP transformation and high flexibility. For faster IMP transformation and reduced process time, multiple copper and tin layers in single preform can also be developed. Here the individual layers must be <15 µm. Here the production of preforms can be extremely difficult, so an irregular stack structure can be expected. Another approach can be according to the HotPowCon concept, where preforms with copper particles can be developed. The process time, wetting characteristics depends on the copper particle percentage filled inside the preform and the used production equipment. The addition of particles in the preform structure is not limited to copper particles but also with new magnetic particles similar to paste based TLPS to enhance and accelerate the IMP formation with shorter process times.

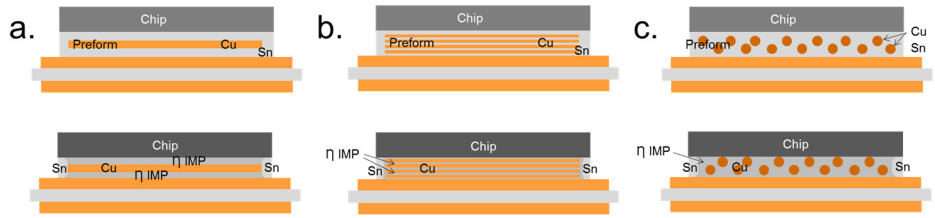


Figure 144: Suggestions on the material development with respect to the preforms. a. Cladded preform structure; b. Multi-layer preforms; c. Preforms with copper particles of sizes according to the bondline.

9 Summary and Outlook

With advances in the new generation WBG semiconductor materials and ever-increasing requirements for reliable power electronic modules at elevated temperatures, a major limitation is the lack of qualified high-temperature device-level packaging. This needs improvement particularly for the high-current and high-voltage power conversion applications. Diffusion soldering is an interconnect technique where high remelting IMPs are produced in the complete bondline by interdiffusion between a HMM (Cu) and a LMM (Sn). The main objective of this thesis work is the optimization and evaluation of Cu-Sn based TLPS, a variant of diffusion soldering to implement as a die-attach technique for power electronics production with high level of flexibility and customization. The approach is to procure a bondline with η-Cu_6Sn_5 IMP as main constituent with remelting temperatures of at least 400 °C between the power electronic components by using Cu-Sn interlayer material.

Firstly as part of the work, the requirements and the trends for the state-of-the-art and advanced power modules obtained from a worldwide conducted survey of 143 participants were summarized. This revealed the importance and requirements of the high-temperature packaging up to 300 °C in various applications and market segments. For the experimental part, the investigations were performed for the paste printing process to attain solder heights down to 20 µm on power electronic substrates. The prepared assemblies using $Sn_{99.3}Cu_{0.7}$ solder pastes were treated thermally to estimate the necessary peak and post-handling process conditions for full IMP transformation. The results are discussed in detail and parallelly compared with a concentration-gradient based 2D-modelling. This lead to requirement of minimum of 18 min peak time in case of copper availability from both substrate and component backside metallization or a minimum of 25 min peak time for copper only from substrates for a total IMP bondline <15 µm. A comprehensive in-situ X-ray analysis was performed to understand the voiding characteristics for the profiles with extended peak-time and pressure variation. Based on all the above preliminary tests, the influential parameters were further modified to investigate the reproducibility and flexibility for defect-free TLPS interconnections.

The feasibility investigations with Cold Active Plasmadust Metallization® (CAPM) technology allowed successful introduction of copper particles into solder depot and also printing sufficient copper on top of solder depot

to enable thicker IMP bondlines. The material-related influential factors modified were mainly paste and preform metal combinations, substrate roughness, component size and metallization. These were combined with the process-related parameters like energy transfer technique, process gas, surrounding pressure and temperature profile (peak temperature, peak time and consecutive thermal treatment). The goal here was to develop an optimized hybrid temperature and pressure profile to obtain low-void TLPS interconnections. The test vehicles were analyzed for IMP thickness and process-generated defects like Kirkendall voids, skeleton formation and the residual flux materials. A comprehensive analysis was performed on the process-related issues of voids for the selected soldering technique and warpage for components of varying dimensions and metallizations.

The over-pressure convection and vacuum vapor-phase soldering systems were mainly used as void-minimizing techniques. A special emphasis was given to the void percentage as the main quality factor. The TLPS assemblies were successfully built using the proposed profile with combination of vacuum and overpressure. The quality of the produced joints was evaluated by thermo-mechanical loading followed by the characterization of thermal and mechanical stability. Destructive shear tests were performed at room and high temperatures up to 450 °C revealed that the paste- and preform based TLPS joints were stable up to 400 °C without loss of adhesion. The assemblies using CAPM however displayed acceptable performance due to presence of rest tin in the bondlines. The average shear strengths obtained were > 50 MPa at 25 °C and approx. 25 MPa at 400 °C. The test assemblies were stable up to 1100 and 2500 thermal cycles of -40 °C/150 °C and -40 °C/125 °C cycles respectively. The observed defects were mainly the increased micro-voids in the interlayer due to usage of the rest tin material for IMC formation and increased Kirkendall voids at ε-Cu_3Sn and Cu-interface leading to crack formation and propagation.

The feasibility of the developed TLPS technology was tested by implementing the materials and optimized temperature profiles for two case studies. Firstly, a product case study for the serial production of silicon based press-pin power packages was successfully performed and demonstrated. Here the Cu-Sn based preforms of various thicknesses developed as part of the work significantly improved the handling and automation of the TLPS technology with high level of product customization. The produced multi-chip TLPS power modules had average void percentages less than 5% with fully transformed η-Cu_6Sn_5 IMP in the bondlines. Secondly, a technology case study was performed for the feasibility of Transient Liquid Phase

Bonding (TLPB, another variant of diffusion soldering) for Sn-Cu and Ag-Sn bimetallic systems with the developed TLPS approach.

Based on the investigations performed as part of this research work, the TLPS interconnects with enriched η Cu_6Sn_5 IMP bondline were realized successfully with optimized solder profiles. It was concluded that the paste-based TLPS assemblies had higher void percentages i.e. 10-15% compared to the preform-based TLPS at < 5%. This was mainly due to the presence of flux materials in the solder pastes for paste-based TLPS. Only few percent in voidrate could be reduced even with enhanced solder profiles with multiple pressure cycles. This however increased the production costs and process-related defects.

The pressure variation strategies for the temperature profiles as introduced in this work significantly improved the quality of the TLPS joints. The consecutive placement of preforms and components highly increases the automation possibility compared to paste-based TLPS. The preform-based concept reduced not only material and production costs but also easier product customization for TLPS.

10 Zusammenfassung und Ausblick

Mit Fortschritten in der neuen Generation von WBG-Halbleitermaterialien und ständig steigenden Anforderungen an die Zuverlässigkeit von Leistungselektronikmodulen bei erhöhten Temperaturen ist eine wesentliche Einschränkung der Mangel an hochtemperaturtauglicher Aufbau- und Verbindungstechnik (AVT). Diese ist insbesondere für Hochstrom- und Hochspannungsumwandlungsanwendungen erforderlich. Diffusionslöten ist eine Verbindungstechnik bei niedrigen Prozesstemperaturen. Dabei werden intermetallische Phasen (IMP) mit hohem Schmelzpunkt durch die Diffusion zwischen einem hochschmelzenden Metall (Cu) und einem niedrigschmelzenden Metall (Sn) in der gesamten Fügezone erzeugt. Das Hauptziel dieser Arbeit ist die Bewertung und Optimierung von Cu-Sn basiertem *Transient Liquid Phase Soldering* (TLPS, eine Variante des Diffusionslötens) als Verbindungstechnik mit hoher Prozessflexibilität und Designanpassung in der Leistungselektronik einzusetzen. Im Rahmen der Arbeit wird eine neuartige Fügezone basierend auf der η-Cu_6Sn_5 intermetallischen Phase untersucht. Diese weist eine hohe Umschmelztemperatur von mindestens 400 °C zwischen den elektronischen Bauelementen bei Verwendung von Cu-Sn Lotmaterial auf.

Zunächst wurden im Rahmen der Arbeit die Anforderungen und die Trends für die hochmodernen und fortschrittlichen Leistungsmodule auf Basis einer weltweiten Umfrage unter 143 Teilnehmern zusammengefasst. Dies zeigte Bedeutung und Anforderungen der Hochtemperatur-AVT bis zu 300 °C in verschiedenen Anwendungen und Marktsegmenten auf. Für den experimentellen Teil wurden zuerst die Untersuchungen für das Pasten-Druckverfahren durchgeführt, um Lotstärken bis zu 20 µm auf keramischen Schaltungsträgern zu erreichen. Die für ein vollständiges Phasenwachstum optimalen Temperaturprofile und Prozessparameter (Peak- und Post-Handling, Anpressdruck, Atmosphäre) wurden anhand vorbereiteter Baugruppen mit $Sn_{99.3}Cu_{0.7}$ Lotpasten ermittelt. Diese Ergebnisse wurden parallel mit denen einer konzentrationsgradientbasierten 2D-Modellierung verglichen. Dies führte für unter 15 µm Fügezone zur Prozessanforderung von mindestens 18 min Peakzeit, wenn sowohl die Substrat als auch die Rückseitenmetallisierung aus Cu besteht, beziehungsweise mindestens 25 min Peakzeit, wenn nur das Substrat eine Cu Metallisierung aufweist. Eine umfassende in-situ Röntgenanalyse wurde durchgeführt, um die Porenreduzierung für Profile mit verlängerter Peakzeit und Atmosphärendruckänderung zu verstehen. Basierend auf allen obigen Vorversuchen

wurden die einflussreichen Parameter weiter optimiert, um die Reproduzierbarkeit und Flexibilität für fehlerfreie TLPS-Verbindungen zu schaffen.

Die Machbarkeitsuntersuchungen mit dem Kupfer-Plasmabeschichtungsverfahren (*Cold Active Plasmadust Metallization*®, CAPM) ermöglichten die erfolgreiche Einbringung von Kupferpartikeln in und auf das Lotdepot, um dickere IMP-Fügezonen zu ermöglichen. Die materialbezogenen Einflussfaktoren waren vor allem Pasten- und Preform-Metallkombinationen, Substratoberflächenrauheit, Bauteilgröße und -metallisierung. Diese wurden mit den prozessbezogenen Parametern wie Energieübertragungstechnik, Prozessgas, Umgebungsdruck, und Temperaturprofil (Peaktemperatur, Peakzeit und thermische Nachbehandlung) kombiniert. Ziel war es, ein optimiertes Hybrid-Temperatur- und Druckprofil zu entwickeln, um porenarme TLPS-Verbindungen zu realisieren. Die Testmuster wurden auf IMP-Dicke und prozessbedingte Defekte wie Kirkendall-Fehlstellen und Skelettbildungen untersucht. Eine umfassende Analyse wurde für prozessbezogene Probleme bezüglich Fehlstellen für die gewählte Löttechnik und Verwölbung für Komponenten unterschiedlicher Abmessungen und Metallisierungen durchgeführt.

Zur Poren-Minimierung wurden hauptsächlich Überdruck-Konvektions- und Vakuum-Dampfphasen-Lötanlagen verwendet. Besonders hervorgehoben wurde der Porenanteil als Hauptqualitätsfaktor. Die postulierte Kombination aus Vakuum und Überdruck im Prozessprofil hatten nachweislich die Defektrate der TLPS-Baugruppen reduziert. Die Qualität der erzeugten Verbindungen wurde durch thermomechanische Stabilitätsuntersuchungen verifiziert. Zerstörende Schertests wurden bei Raum- und Hochtemperaturen bis zu 450 °C durchgeführt. Diese Tests zeigten, dass die pasten- und preformbasierten TLPS-Verbindungen bis zu 400 °C ohne Haftungsverlust stabil waren. Die Baugruppen, die CAPM verwendeten, zeigten jedoch geringere Haftfestigkeiten aufgrund des Vorhandenseins von Restzinn in den Verbindungen. Die erzielten mittleren Scherfestigkeiten betrugen über 50 MPa bei 25 °C und ca. 25 MPa bei 400 °C. Die Baugruppen waren bis zu 1100 und 2500 thermischen Zyklen von -40 °C/150 °C bzw. -40 °C/125 °C Zyklen stabil. Die beobachteten Defekte waren vor allem die erhöhte Anzahl von Mikroporen aufgrund der Verwendung des Rest-Zinnmaterials für das Phasenwachstum in der Fügezone und erhöhte Kirkendall-Fehlstellen bei ε-Cu_3Sn und Cu-Grenzflächen, die zu Rissbildung und -ausbreitung führten.

Der entwickelte TLPS-Ansatz wurde durch die Umsetzung der Materialien und der optimierten Prozessbedingungen anhand zweier Fallstudien getestet: Zunächst wurde eine Produktfallstudie für die Serienproduktion von siliziumbasierten Press-Pin-Modulen erfolgreich durchgeführt. Hier haben die Cu-Sn-basierten Preforms verschiedener Dicken, die im Rahmen der Arbeit entwickelt wurden, die Handhabung und Automatisierung der TLPS-Technologie deutlich verbessert. Die produzierten Multi-Chip-TLPS-Leistungsmodule hatten durchschnittliche Defektraten von weniger als 5% bei vollständig transformierten η-Cu_6Sn_5 IMP in den Fügezonen. Zweitens wurde eine Technologiefallstudie für die Machbarkeit einer zweiten Diffusionslotvariante (*Transient Liquid Phase Bonding*, TLPB) für Sn-Cu- und Ag-Sn Bimetallsysteme mit dem entwickelten TLPS-Ansatz durchgeführt.

Basierend auf den im Rahmen dieser Forschungsarbeit durchgeführten Untersuchungen wurden die TLPS-Verbindungen mit angereicherten η-Cu_6Sn_5 IMP erfolgreich mit optimierten Lötprofilen realisiert. Es wurde festgestellt, dass die pastenbasierten TLPS-Baugruppen höhere Porenanteile von 10-15% im Vergleich zu preformbasierten TLPS-Baugruppen mit <5% Porenanteilen hatten. Dies war vor allem auf das Vorhandensein von Flussmittel in den Lotpasten bei den pasten-basierten TLPS-Baugruppen zurückzuführen. Hier konnten auch bei angepassten Lötprofilen mit mehreren Druckzyklen die Lunkerraten nur minimal reduziert werden. Dies erhöhte jedoch einerseits die Produktionskosten, andererseits die prozessbedingten Defektraten.

Die Druckvariationsstrategien für die in dieser Arbeit eingeführten Temperaturprofile haben die Qualität der TLPS-Verbindungen deutlich verbessert. Die aufeinanderfolgende Bestückung von Preforms und Komponenten während des Herstellungsprozesses ermöglichte die Erhöhung des Automatisierungsgrades im Vergleich zur pastenbasierten TLPS. Der preformbasierte Ansatz reduziert nicht nur die Material- und Herstellungskosten, sondern erleichtert auch eine Produktanpassung für TLPS.

Bibliography

[1] N.N.: World Energy Outlook 2016 - Executive Summary - English version. International Energy Agency. URL http://www.iea.org/publications/freepublications/publication/WorldEnergyOutlook2016ExecutiveSummaryEnglish.pdf, (Access date: 15.12.2016)

[2] N.N.: World Energy Scenarios: Composing energy futures to 2050. World Energy Council, (Access date: 21.10.2015)

[3] ECPE European Center for Power Electronics e.V.; EPE European Power Electronics and Drives Association: Energy Efficiency - The Role of Power Electronics. ECPE Position Paper. URL http://www.ecpe.org/securedl/0/1482335878/25edf33f5bd557273cfe1c63b6eb14775b1ee945/fileadmin/user_upload/Roadmaps___Strategy_Papers/ECPE_Position_Paper_Energy_Efficiency.pdf, (Access date: 01.05.2014)

[4] ECPE European Center for Power Electronics e.V.: Electronics for Energy Efficiency and Sustainability (EEESy): The Strategic Research Initiative for Efficient Electric Power Conversion. URL http://www.ecpe.org/securedl/0/1482335878/d66a4f3fce8fd8113c745079c2e6e2f0d2b25b37/fileadmin/user_upload/Roadmaps___Strategy_Papers/ECPE_Strategic_Research_Agenda__EEESy.pdf, (Access date: 15.06.2014)

[5] LIPSKY, J.: Power Electronics Market Surges: Electric vehicles help drive growth. URL http://www.eetimes.com/document.asp?doc_id=1326345, (Access date: 10.07.2015)

[6] KOLAR, J. W.; HOENE, E.; HARDER, T.: Vision: Roadmap Power Electronics 2025. In: ECPE European Center for Power Electronics e.V. (ed.): ECPE Roadmap: Power Electronics 2025. Nuremberg, 2015

[7] TRIVEDI, M.; SHENAI, K.: High temperature capability of devices on Si and wide bandgap materials. In: Conference Record of 1998 IEEE Industry Applications Conference. Thirty-Third IAS Annual Meeting (Cat. No.98CH36242) Vol. 2 (1998), p. 959–962

[8] KHAZAKA, R.; MENDIZABAL, L.; HENRY, D.; HANNA, R.: Survey of High-Temperature Reliability of Power Electronics Packaging Components. In: IEEE Transactions on Power Electronics Vol. 30 (2015), Nr. 5, p. 2456–2464

[9] CHANG, S. S.; PANKOVE, J.; LEKSONO, M.; VAN ZEGHBROECK, B.: 500°C operation of a GaN/SiC heterojunction bipolar transistor. In: MISHRA, U. K. (ed.): 1995 53rd Annual Device Research Conference digest: June 19-21, 1995, University of Virginia, Charlottesville, Virginia. [New York]: IEEE Electron Devices Society, 1995, p. 106–107

[10] CASADY, J. B.; DILLARD, W. C.; JOHNSON, R. W.; RAO, U.: A hybrid 6H-SiC temperature sensor operational from 25°C to 500°C. In: IEEE Transactions on Components, Packaging, and Manufacturing Technology: Part A Vol. 19 (1996), Nr. 3, p. 416–422

[11] CONNET, D.: Integration and Miniaturization Trends: Passive embedding for performance and reliability. URL https://www.semikron.com/dl/service-support/downloads/download/semikron-technical-articles-skin-technology-for-ultra-compact-power-modules-en-2012-09-19, (Access date: 01.10.2013)

[12] SHAMMAS, N.: Present problems of power module packaging technology. In: Microelectronics Reliability Vol. 43, 2003, Nr. 4, p. 519–527

[13] CHELNOKOV, V. E.; SYRKIN, A. L.: High temperature electronics using SiC: Actual situation and unsolved problems. In: Materials Science and Engineering: B Vol. 46 (1997), 1-3, p. 248–253

[14] DÉPLANQUE, S.: Lifetime prediction for solder die-attach in power applications by means of primary and secondary creep. Technische Universität Cottbus-Senftenberg, Fakultät für Maschinenbau, Elektrotechnik und Wirtschaftsingenieurwesen (eBTU) / LS Konstruktion und Fertigung: Doctoral thesis. 2007

[15] MATIJASEVIC, G. S.; WANG, C. Y.; LEE, C. C.: Thermal Stress Considerations in Die-Attachment. In: LAU, J. H. (ed.): Thermal stress and strain in microelectronics packaging. New York: Van Nostrand Reinhold, 1993, p. 194–220

[16] GUTH, K.; HEUCK, N.; STAHLHUT, C.; CILIOX, A.; OESCHLER, N.; BOEWER, L.; TOPHINKE, S.; BOLOWSKI, D.; SPECKELS, R.; KERSTING, C.; KRASEL, S.; STROTMANN, G.: End-of-life investigation on the .XT interconnect technology. Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management

[17] GUTH, K.; OESCHLER, N.; Boewer. L.; SPECKELS, R.; STROTMANN, G.; HEUCK, N.; KRASEL, S.; CILIOX, A.: New assembly and interconnect technologies for power modules. In: 2012 7th International Conference on Integrated Power Electronics Systems (CIPS), 2012, p. 1–5

[18] GRASSHOFF, T.: SKiN Technology for Ultra Compact Power Modules. URL https://www.semikron.com/dl/service-support/downloads/download/semikron-technical-articles-skin-technology-for-ultra-compact-power-modules-en-2012-09-19, (Access date: 01.02.2015)

[19] HUMPSTON, G.; JACOBSON, D.; SANGHA, S.: Diffusion soldering for electronics manufacturing. In: Endeavour Vol. 18 (1994), Nr. 2, p. 55–60

[20] WINTRICH, A.; NICOLAI, U.; TURSKY, W.; REIMANN, T.: Applikationshandbuch Leistungshalbleiter. 2. Ed. Betriebsstätte des ISLE e.V: ISLE Verlag, 2015

[21] LITTLE, A.: Leistungselektronik Automotive 2015: Markt- und Technologiestudie. URL http://www.adlittle.de/studien.html?view=175, (Access date: 01.06.2016)

[22] LIU, Y.: Power electronic packaging: Design, assembly process, reliability and modeling. New York: Springer, 2012

[23] SCHULZ-HARDER, J.: DBC substrates as a base for power MCM's. In: LIM, T. B.; LEE, C.; TOH, K. C. (ed.): 3rd Electronics Packaging Technology Conference. Piscataway, N.J.: IEEE, 2000, p. 315–320

[24] SCHULZ-HARDER, J.; EXEL, K.: Recent developments of direct bonded copper (DBC) substrates for power modules. In: IEEE (ed.): 5th International Conference on EPTC/ ICEPT, 2003, p. 491–496

[25] VOELLER, U.; LEHMEIER, B.: Silicon Nitride Substrates for Power Electronics. URL http://blog.rogerscorp.com/wp-content/uploads/2013/03/Rogers_ Si3N4_DCB_AMB_20130117.pdf (Access date: 15.08.2016)

[26] KOLLENBERG, W. (Ed.): Technische Keramik: Grundlagen, Werkstoffe, Verfahrenstechnik. 2. Ed. Essen: Vulkan-Verl., 2009

[27] WEIDNER, K.; KASPAR, M.; SELIGER, N.: Planar Interconnect Technology for Power Module System Integration. 7th International Conference on Integrated Power Electronics Systems (CIPS) (2012)

[28] PLOSS, R.: IFX Day 2011. URL http://www.infineon.com/dgdl/3FXDay2011_Ploss.pdf?folderId=db3a30432f549109012f54c3ec1e0002&fileId=db3a304330046413013066e8a42d409a, (Access date: 15.09.2016)

[29] N.N.: SKiN flex layers replace wire bonding. URL https://www.semikron.com/innovation-technology/construction-and-connection-technology/skin-technology.html, (Access date: 01.10.2016)

[30] SCHEUERMANN, U.: Reliability of Planar SKiN Interconnect Technology. In: VDE (ed.): 2012 7th International Conference on Integrated Power Electronics Systems (CIPS), 2012

[31] N.N.: IGBT modules with internal inductance of just 15nH. URL http://www.electricalmonitor.com/PrintArticle.aspx?aid=255, (Access date: 21.06.2014)

[32] N.N.: Infineon Technologies: Infineon power modules for hybrid and electric vehicles help meet space constraints and deliver higher power density: HybridPACK™ DSC (Double Sided Cooling). URL http://www.infineon.com/cms/en/about-infineon/press/market-news/2016/INFATV201605-056.html, (Access date: 15.05.2016)

[33] JACKSON, B.: Bond Wireless Building Blocks Provide a New Approach to Power Modules. URL http://www.infineon.com/dgdl/1009pee1303.pdf?fileId=5546d4625336600a40153569250032b59 (Access date: 25.05.2015)

[34] STEVANOVIC, L.: Packaging Challenges and Solutions for Silicon Carbide Power Electronics. URL https://www.ectc.net/files/62/3_2_Stevanovic_GE.pdf (Access date: 30.11.2016)

[35] ANWAR, M.; HAYES, M.; TATA, A.; TEIMORZADEH, M.; ACHATZ, T.: Power Dense and Robust Traction Power Inverter for the Second-Generation Chevrolet Volt Extended-Range EV. In: SAE International Journal of Alternative Powertrains Vol. 4 (2015), Nr. 1, p. 145–152

[36] N.N: APSI3D Raises €1.5 million seed to produce innovative power modules. URL http://www.pointthepower.com/apsi3d-raises-e1-5-million-seed-to-produce-innovative-power-modules, (Access date 15.10.2015)

[37] OGAWA, K.: Toyota Cuts PCU Cost by 30% for New Prius. URL http://techon.nikkeibp.co.jp/atclen/news_en/15mk/120200210, (Access date: 10.08.2016)

[38] HARDER, T.: ECPE Roadmap Workshop 2014: Power Electronics 2025. In: ECPE European Center for Power Electronics e.V. (ed.): ECPE Roadmap: Power Electronics 2025. Nuremberg, 2015

[39] ZVEI - Zentralverband Elektrotechnik- und Elektronikindustrie e.V.: ZVEI: Technologie Roadmap Stressarme MST-Packages: Trends, Perspektiven, Herausforderungen

[40] N.N.: iNEMI 2015 Roadmap: Advanced manufacturing technology

[41] PFAHL, B.; FU, H.; RICHARDSON, C.: Highlights of iNEMI 2013 technology roadmaps. In: 35th IEEE. Piscataway, NJ: IEEE, 2012, p. 1–5

[42] N.N.: IPC: 2015 International Technology Roadmap for Electronic Interconnections

[43] MOORE, G. E.: Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff. In: IEEE Solid-State Circuits Newsletter Vol. 20 (2006), Nr. 3, p. 33–35

[44] BALIGA, B. J.: Fundamentals of power semiconductor devices. New York: Springer, 2008

[45] CIAPPA, M.: Selected failure mechanisms of modern power modules. In: Microelectronics Reliability Vol. 42 (2002), 4-5, p. 653–667

[46] KRAUSSE, D.: High power AlGaN/GaN HFETs for industrial, scientific and medical applciations. University of Freiburg, Germany: Doctoral thesis. 2013

[47] HORNERGER, J.; LOSTETTER, A. B.; OLEJNICZAK, K. J.; MCNUTT, T.; LAL, S. M.; MANTOOTH, A.: Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments. In: WILLIAMSON, D. A. (ed.): 2005 IEEE Aerospace Conference proceedings: March 5-12, 2005, Big Sky, MT. Piscataway, N.J.: IEEE, 2004, p. 2538–2555

[48] BARLOW, F. D.; ELSHABINI, A.: High-Temperature High-Power Packaging Techniques for HEV Traction Applications, 2007

[49] HUTZLER, A.; TOKARSKI, A.; KRAFT, S.; ZISCHLER, S.; SCHLETZ, A.: Increasing the lifetime of electronic packaging by higher temperatures: Solders vs. silver sintering. In: IEEE 64th Electronic Components and Technology Conference (ECTC), 2014: 27-30 May 2014, Lake Buena Vista, Orlando, Florida, USA. Piscataway, NJ: IEEE, 2014, p. 1700–1706

[50] HAGLER, P.; HENSON, P.; JOHNSON, R. W.: Packaging Technology for Electronic Applications in Harsh High-Temperature Environments. In: IEEE Transactions on Industrial Electronics Vol. 58 (2011), Nr. 7, p. 2673–2682

[51] COPPOLA, L.; HUFF, D.; WANG, F.; BURGOS, R.; BOROYEVICH, D.: Survey on High-Temperature Packaging Materials for SiC-Based Power Electronics Modules. In: 2007 IEEE Power Electronics Specialists Conference (PESC07). Piscataway, N.J.: IEEE, 2007, p. 2234–2240

[52] ECPE European Center for Power Electronics e.V. (Ed.): ECPE Roadmap: Power Electronics 2025. Nuremberg, 2015

[53] N.N.: RoHS: Restriction of Hazardous Substances Directive: EU Law and publications. URL http://eur-lex.europa.eu/LexUriServ/LexUriServ.do?uri=CELEX:32002L0096:EN:NOT, (Access date: 13.06.2013)

[54] N.N.: WEEE: Waste Electrical and Electronic Equipment Directive: EU Law and publications. URL http://eur-lex.europa.eu/legal-content/EN/ALL/?uri=CELEX:32002L0095, (Access date: 13.06.2013)

[55] LEE, N.-C.: Reflow soldering processes and troubleshooting: SMT, BGA, CSP and flip chip technologies. Boston [u.a.]: Newnes, 2002

[56] LEE, C. C.; WANG, P. J.; KIM, J. S.: Are Intermetallics in Solder Joints Really Brittle? In: 2007 IEEE 57th Electronic Components & Technology Conference: Sparks, NV : 29 May - June 1, 2007. Piscataway, N.J.: IEEE, 2007, p. 648–652

[57] BELL, H.: Reflowlöten Grundlagen, Verfahren, Temperaturprofile und Lötfehler, Eugen G: Leuze Verlag Bad Saulgau, ISBN, 2005

[58] WOLTER, K. J.;ZERNA, T.;DETERT, M. (Eds.): Ewald, Thomas D.: Untersuchungen zum Mechanismus der Porenentstehung in Weichlotverbindungen beim Reflowlöten. 1. Ed. Templin: Detert, 2013

[59] KOCH, J.; STARZ, K. A.; SCHAEFER, G.; KUEHNHOLD, H.: Weichlotpaste zum Löten von elektronischen Schaltungen. Patent Nr. DE4235575C2

[60] ASPANDIAR, R. F.: Voids in solder joints. In: Journal of SMT Article Vol. 19 (2006), Nr. 4

[61] FREAR, D. R.; JANG, J. W.; LIN, J. K.; ZHANG, C.: Pb-free solders for flip-chip interconnects. In: JOM Vol. 53 (2001), Nr. 6, p. 28–33

[62] HANCE, W. B.; LEE, N. C.: Voiding Mechanisms in SMT. In: Soldering & Surface Mount Technology Vol. 5 (1993), Nr. 1, p. 16–21

[63] KIM, S.; KIM, K.-S.; KIM, S.-S.; SUGANUMA, K.; IZUTA, G.: Improving the Reliability of Si Die Attachment with Zn-Sn-Based High-Temperature Pb-Free Solder Using a TiN Diffusion Barrier. In: Journal of Electronic Materials Vol. 38 (2009), Nr. 12, p. 2668–2675

[64] Panasonic: Quality and Reliability Information. URL http://www.semicon.panasonic.co.jp/en/aboutus/reliability.html, (Access date: 01.10.2013)

[65] LUCAS, J. P.; RHEE, H.; GUO, F.; SUBRAMANIAN, K. N.: Mechanical properties of intermetallic compounds associated with Pb-free solder joints using nanoindentation. In: Journal of Electronic Materials Vol. 32 (2003), Nr. 12, p. 1375–1383

[66] SUNSHINE, R. A.; D'AIELLO, R. V.: Direct observation of the effect of solder voids on the current uniformity of power transistors. In: IEEE Transactions on Electron Devices Vol. 22 (1975), Nr. 2, p. 61–62

[67] DIN EN 61190-1-1:2003-01. Attachment materials for electronic assembly - Part 1-1: Requirements for soldering fluxes for high-quality interconnections in electronics assembly (IEC 61190-1-1:2002). 2013

[68] SCHRÖDER, D.: Leistungselektronische Bauelemente. 2. Aufl. Berlin, Heidelberg: Springer-Verlag Berlin Heidelberg, 2006

[69] TARR, M.: The 'homologous' temperature. URL http://www.mtarr.co.uk/courses/topics/index.asp., (Access date: 05.10.2015)

[70] NEUDECK, P. G.; OKOJIE, R. S.; CHEN, L.-Y.: High-temperature electronics - a role for wide bandgap semiconductors? In: Proceedings of the IEEE Vol. 90 (2002), Nr. 6, p. 1065–1076

[71] OHADI, M.; QI, J.: Thermal Management of Harsh-Environment Electronics, Bd. 193. In: KAKAÇ, S. (ed.): Microscale heat transfer: Fundamentals and applications. Dordrecht: Springer in association with NATO Public Diplomacy Division, 2005 (NATO science series. Series II, Mathematics, physics, and chemistry, v. 193), p. 479–498

[72] HENSON, P. E.: Considerations and options for high temperature die attach. Auburn University, Auburn, Alabama, USA: Master thesis. 2010

[73] GUTH, K.; SIEPE, D.; GÖRLICH, J.; TORWESTEN, H.; ROTH, R.; HILLE, F.; UMBACH, F.: New assembly and interconnects beyond sintering methods. In: Proceedings of PCIM Europe, 2010, p. 232–237

[74] JIANG, L.: Thermo-mechanical reliability of sintered-silver joint versus lead-free solder for attaching large-area devices. Virginia Polytechnic Institute and State University, Blacksburg, Virginia, USA: Master thesis. 2010

[75] GOEBL, C.; FALTENBACHER, J.: Low temperature sinter technology die attachment for power electronic applications. 6th International Conference on Integrated Power Electronics Systems, 2010

[76] ZHANG, Z.: Processing and characterization of micro-scale and nanoscale silver. Virginia Polytechnic Institute and State University, Balcksburg, Virginia, USA: Doctoral thesis. 2005

[77] Die attach of power devices using silver sintering- Bonding process optimization and characterization, 2011

[78] BAJWA, A. A.; ZEISER, R.; WILDE, J.: Process optimization and characterization of a novel micro-scaled silver sintering paste as a die-attach material for high temperature high power semiconductor devices. In: 36th International Spring Seminar on Electronics Technology (ISSE)-Automotive Electronics. Piscataway, N.J.: IEEE, 2013, p. 53–58

[79] SYED-KHAJA, A.; HOERBER, J.; GRUBER, C.; FRANKE, J.: A novel approach for thin-film Ag-sintering process through Aerosol Jet Printing in power electronics. In: 2015 European Microelectronics Packaging Conference (EMPC), 2015

[80] BAI, J. G.; ZHANG, Z. Z.; CALATA, J. N.; LU, G.-Q.: Low-Temperature Sintered Nanoscale Silver as a Novel Semiconductor Device-Metallized Substrate Interconnect Material. In: IEEE Transactions on Components and Packaging Technologies Vol. 29 (2006), Nr. 3, p. 589–593

[81] BAI, J.; ZHANG, Z.; CALATA, J.; LU, G.-q.: Characterization of Low-Temperature Sintered Nanoscale Silver Paste for Attaching Semiconductor Devices. In: High density microsystem design and packaging and component failure analysis. [New York]: IEEE, 2004, p. 1–5

[82] SIOW, K. S.: Are Sintered Silver Joints Ready for Use as Interconnect Material in Microelectronic Packaging? In: Journal of Electronic Materials Vol. 43 (2014), Nr. 4, p. 947–961

[83] KÄHLER, J.: Entwicklung eines Sinterverfahrens zur Chipmontage von Bauelementen und Sensoren für Hochtemperatur-Elektronik. 1. Ed. München: Dr. Hut, 2012

[84] BAI, J. G.; CALATA, J. N.; LU, G.-Q.: Processing and Characterization of Nanosilver Pastes for Die-Attaching SiC Devices. In: IEEE Transactions on Electronics Packaging Manufacturing Vol. 30 (2007), Nr. 4, p. 241–245

[85] BADER, S.: Erzeugung thermisch stabiler Mikroverbindungen durch isotherme Erstarrung. Stuttgart, Universität Stuttgart, Institut für Metallkunde: Doctoral thesis. 1990

[86] PANCHENKO, I.: Process-dependent microstructure changes in solid-liquid interdiffusion interconnects for 3D integration / Iuliana Panchenko. 1. Aufl. Templin: Detert, 2014

[87] BERNSTEIN, L.: Semiconductor Joining by the Solid-Liquid-Interdiffusion (SLID) Process: I. The Systems Ag-In, Au-In, and Cu-In. In: Journal of The Electrochemical Society Vol. 113 (1966), Nr. 12, p. 1282–1288

[88] MANIKAM, V. R.; CHEONG, K. Y.: Die Attach Materials for High Temperature Applications: A Review. In: IEEE Transactions on Components, Packaging and Manufacturing Technology Vol. 1 (2011), Nr. 4, p. 457–478

[89] JIANG, L.: Electrical and thermal characterizations of IGBT module with pressure-free large-area sintered joints. Virginia Polytechnic Institute and State University, Blacksburg, Virginia, USA: Master thesis. 2013

[90] ABTEW, M.; SELVADURAY, G.: Lead-free Solders in Microelectronics. In: Materials Science and Engineering: R: Reports Vol. 27 (2000), 5-6, p. 95–141

[91] CHROMIK, R. R.; VINCI, R. P.; ALLEN, S. L.; NOTIS, M. R.: Measuring the mechanical properties of Pb-free solder and Sn-based intermetallics by nanoindentation. In: JOM Vol. 55 (2003), Nr. 6, p. 66–69

[92] SONG, J.-M.; LU, W.-C.: Phase evolution and nanomechanical properties of intermetallic compounds in solid-liquid interdiffusion bonding. In: 2014 International Conference on Electronics Packaging (ICEP): IEEE, 2014, p. 640–643

[93] DENG, X.; CHAWLA, N.; CHAWLA, K.; KOOPMAN, M.: Deformation behavior of (Cu, Ag)–Sn intermetallics by nanoindentation. In: Acta Materialia Vol. 52 (2004), Nr. 14, p. 4291–4303

[94] KUMAR, S.; JUNG, J.: Mechanical and electronic properties of Ag3Sn intermetallic compound in lead free solders using ab initio atomistic calculation. In: Materials Science and Engineering: B Vol. 178 (2013), Nr. 1, p. 10–21

[95] HERBOTH, T.; GUENTHER, M.; ZEISER, R.; WILDE, J.: Investigation of stress states in silicon dies induced by the Low Temperature Joining Technology. In: 14th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), 2013. Piscataway, NJ: IEEE, 2013, p. 1–6

[96] COOK, G. O.; SORENSEN, C. D.: Overview of transient liquid phase and partial transient liquid phase bonding. In: Journal of Materials Science Vol. 46 (2011), Nr. 16, p. 5305–5323

[97] NATSUME, Y.; OHSASA, K.; NARITA, T.: Phase-field Simulation of Transient Liquid Phase Bonding Process of Ni Using Ni-P Binary Filler Metal. In: MATERIALS TRANSACTIONS Vol. 44 (2003), Nr. 5, p. 819–823

[98] ARAFIN, M. A.; MEDRAJ, M.; TURNER, D. P.; BOCHER, P.: Transient liquid phase bonding of Inconel 718 and Inconel 625 with BNi-2: Modeling and experimental investigations. In: Materials Science and Engineering: A Vol. 447 (2007), 1-2, p. 125–133

[99] CHUANG, R. W.; LEE, C. C.: Silver-indium joints produced at low temperature for high temperature devices. In: IEEE Transactions on Components and Packaging Technologies Vol. 25 (2002), Nr. 3, p. 453–458

[100] FREAR, D. R.; VIANCO, P. T.: Intermetallic growth and mechanical behavior of low and high melting temperature solder alloys. In: Metallurgical and Materials Transactions A Vol. 25 (1994), Nr. 7, p. 1509–1523

[101] MCNULTY, J. C.: Processing and reliability issues for eutectic AuSn solder joints. In: Proceedings of 41th International Symposium on Microelectronics (IMAPS), 2008, p. 909–916

[102] WELCH, W.; CHAE, J.; LEE, S.-H.; YAZDI, N.; NAJAFI, K.: Transient liquid phase (TLP) bonding for microsystem packaging applications. In: Transducers '05: 13th International Conference on Solid-State Sensors, Actuators, and Microsystems : digest of technical papers : June 5-9, 2005. Piscataway, NJ: IEEE, 2005, p. 1350–1353

[103] WILDE, J.; PCHALEK, N.: Kontaktierung von Solarzellen durch isotherme Erstarrung: Telefunken, 1992

[104] LI, J. F.; AGYAKWA, P. A.; JOHNSON, C. M.: Kinetics of Ag3Sn growth in Ag–Sn–Ag system during transient liquid phase soldering process. In: Acta Materialia Vol. 58, 2010, Nr. 9, p. 3429–3443

[105] MUSTAIN, H. A.; BROWN, W. D.; ANG, S. S.: Transient Liquid Phase Die Attach for High-Temperature Silicon Carbide Power Devices. In: IEEE Transactions on Components and Packaging Technologies Vol. 33 (2010), Nr. 3, p. 563–570

[106] HOERBER, J.; GOTH, C.; FRANKE, J.; HEDGES, M.: Electrical functionalization of thermoplastic materials by Aerosol Jet Printing. In: IEEE 13th Electronics Packaging Technology Conference (EPTC), 2011: 7 - 9 Dec. 2011, Singapore. Piscataway, NJ: IEEE, 2011, p. 813–818

[107] BAI, G.: Low-temperature sintering of nanoscale silver paste for semiconductor. Virginia Polytechnic Institute and State University, Blacksburg, Virginia, USA: Doctoral thesis. 2005

[108] SCHMITT, W.: Novel silver contact paste lead free solution for die attach. 2010 6th International Conference on Integrated Power Electronics Systems, 2010

[109] LUTZ, J.; H. Schlangenotto; U. Scheuermann; R. De Doncker: Semiconductor power devices: Physics, characteristics, reliability. Berlin u.a.: Springer, 2011

[110] SCHEUERMANN, U.: Extension of operation temperature range to 200°C enabled by. URL https://www.semikron.com/dl/service-support/downloads/download/semikron-technical-articles-extension-of-operation-temperature-range-to-200c-en-2012-06-19, (Access date: 01.03.2014)

[111] ZEISER, R.; WAGNER, P.; WILDE, J.: Investigation of ultrasonic platinum and palladium wire bonding as interconnection technology for high-temperature SiC-MEMS. In: 2012 4th Electronics System-Integration Technology Conference: 17-20 September 2012, Amsterdam, Netherlands. [Piscataway, N.J.]: IEEE, 2012, p. 1–6

[112] JINKA, K. K.: Thermo-mechanical analysis of encapsulted ball-wedge wire bonds. University of Maryland, College Park: Master thesis. 2006

[113] AMRO, R.: Power cycling capability of advanced packaging and interconnection technologies at high temperature swings. Techn. University of Chemnitz: Doctoral thesis. 2006

[114] KAESTLE, C.; SYED-KHAJA, A.; REINHARDT, A.; FRANKE, J.: Investigations on ultrasonic copper wire wedge bonding for power electronics. In: 36th International Spring Seminar on Electronics Technology (ISSE)-Automotive Electronics. Piscataway, N.J.: IEEE, 2013, p. 79–84

[115] KÄSTLE, C.; FRANKE, J.: Comparative Analysis of the Process Window of Aluminum and Copper Wire Bonding for Power Electronics Applications. In: Proceedings of the 2014 International Conference on Electronics Packaging (ICEP). Tokyo, 2014, p. 335–340

[116] SYED-KHAJA, A.; KAESTLE, C.; FRANKE, J.: Reliable packaging technologies for power electronics: Diffusion soldering and heavy copper wire bonding. In: 3rd International Electric Drives Production Conference (EDPC): IEEE, 2013, p. 1–6

[117] SCHEUERMANN, U.: Packaging and Reliability of Power Modules - Principles, Achievements and Future Challenges. Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2015

[118] SCHEUERMANN, U.; SCHMIDT, R.: A new lifetime model for advanced power modules with sintered chips and optimized Al wire bonds, 2013

[119] CHANG, T.-C.; CHANG, J.-Y.; CHUANG, T.-H.; Lo Wei-Chung: Dual-phase solid-liquid interdiffusion bonding, a solution for the die attachment of WBG. In: 2012 14th International Conference on Electronic Materials and Packaging (EMAP). Red Hook, NY: Curran, 2012, p. 1–5

[120] N.N.: TLP Library: Diffusion mechanisms. URL https://www.doitpoms.ac.uk/tlplib/diffusion/diffusion_mechanism.php, (Access date: 25.08.2016)

[121] LAURILA, T.; VUORINEN, V.; KIVILAHTI, J. K.: Interfacial reactions between lead-free solders and common base materials. In: Materials Science and Engineering: R: Reports Vol. 49 (2005), 1-2, p. 1–60

[122] N.N.: What Is Diffusion? - COMSOL Multiphysics®: Multiphysics Cyclopedia. URL https://www.comsol.fr/multiphysics/what-is-diffusion, (Access date: 12.10.2015)

[123] MACDONALD, W. D.; EAGAR, T. W.: Transient Liquid Phase Bonding. In: Annual Review of Materials Science Vol. 22 (1992), Nr. 1, p. 23–46

[124] SAHA, R. K.; KHAN, T. I.: Effect of bonding variables on TLP bonding of oxide dispersion strengthened superalloy. In: Journal of Materials Science Vol. 42 (2007), Nr. 22, p. 9187–9193

[125] WU, X.; CHANDEL, R. S.; LI, H.: Evaluation of transient liquid phase bonding between nickel-based superalloys. In: Journal of Materials Science Vol. 36 (2001), Nr. 6, p. 1539–1546

[126] KWON, Y.-S.; KIM, J.-S.; MOON, J.-S.; SUK, M.-J.: Transient liquid phase bonding process using liquid phase sintered alloy as an interlayer material. In: Journal of Materials Science Vol. 35 (2000), Nr. 8, p. 1917–1924

[127] MACDONALD, W. D.: Kinetics of transient liquid phase bonding. Massachusetts Institute of Technology: Doctoral thesis. 1993

[128] KHAN, T. I.; WALLACH, E. R.: Transient liquid-phase bonding of ferritic oxide dispersion strengthened superalloy MA957 using a conventional nickel braze and a novel iron-base foil. In: Journal of Materials Science Vol. 30, 1995, Nr. 20, p. 5151–5160

[129] N.N.: Infineon Technologies: Infineon bietet 100 Prozent bleifreie Leistungs-MOSFETs in Standard-TO-Gehäusen für die Automobilindustrie. URL http://www.infineon.com/cms/de/about-infineon/press/market-news/2011/INFATV201112-014.html, (Access date: 05.06.2013)

[130] NOWOTTNICK, M.;WILDE, J.;PAPE, U. (Eds.): Neue Reflowlöttechnologie für elektronische Anwendungen bis 300°C. 1. Ed. Templin: Detert, M, 2014

[131] SYED-KHAJA, A.; KAESTLE, C.; REINHARDT, A.; FRANKE, J.: Optimized thin-film diffusion soldering for power-electronics production. In: 36th International Spring Seminar on Electronics Technology (ISSE)-Automotive Electronics. Piscataway, N.J.: IEEE, 2013, p. 11–16

[132] EHRHARDT, C.; HUTTER, M.; OPPERMANN, H.; LANG, K.-D.: A lead free joining technology for high temperature interconnects using Transient Liquid Phase Soldering (TLPS). In: IEEE 64th Electronic Components and Technology Conference (ECTC), 2014: 27-30 May 2014, Lake Buena Vista, Orlando, Florida, USA. Piscataway, NJ: IEEE, 2014, p. 1321–1327

[133] EHRHARDT, C.; HUTTER, M.; WEBER, C.; LANG, K. D.: Active power cycling results using copper tin TLPB joints as new die-attach technology. Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2015

[134] STROGIES, J.; WILKE, K.: Universal high-temperature suitable joint adapting diffusion soldering. In: Electronics System-Integration Technology Conference (ESTC), 2014: 16-18 Sept. 2014, Helsinki. Piscataway, NJ: IEEE, 2014, p. 1–7

[135] LIN, D.; WANG, G.; SRIVATSAN, T.; AL-HAJRI, M.; PETRAROLI, M.: The influence of copper nanopowders on microstructure and hardness of lead–tin solder. In: Materials Letters Vol. 53 (2002), 4-5, p. 333–338

[136] CHOI, S.; LEE, J. G.; GUO, F.; BIELER, T. R.; SUBRAMANIAN, K. N.; LUCAS, J. P.: Creep properties of Sn-Ag solder joints containing intermetallic particles. In: JOM Vol. 53 (2001), Nr. 6, p. 22–26

[137] WEIS, S.: Beitrag zur Entwicklung partikelverstärkter Weich- und Weichaktivlote zum Fügen temperaturempfindlicher Aluminium-matrix-Verbundwerkstoffe. Chemnitz, Technische Universität Chemnitz, Institut für Werkstoffwissenschaft und Werkstofftechnik: Doctoral thesis, 2012

[138] GUO, F.; CHOI, S.; LUCAS, J. P.; SUBRAMANIAN, K. N.: Microstructural characterisation of reflowed and isothermally-aged Cu and Ag particulate reinforced Sn-3.5Ag composite solders. In: Soldering & Surface Mount Technology Vol. 13 (2001), Nr. 1, p. 7–18

[139] GREVE, H.; CHEN, L.-Y.; FOX, I.; MCCLUSKEY, F. P.: Transient liquid phase sintered attach for power electronics. In: IEEE 63rd Electronic Components and Technology Conference (ECTC), 2013. Piscataway, NJ: IEEE, 2013, p. 435–440

[140] GREVE, H.; MCCLUSKEY, F. P.: Reliability of Sn based LT-TLPS Joints for High Temperature Electronic Systems. CIPS 2014; 8th International Conference on Integrated Power Electronics Systems, 2014

[141] EHRHARDT, C.: Transient Liquid Phase Soldering als Verbindungstechnik leistungselektronischer Halbleiter für Hochtemperaturanwendungen. Berlin, Technische Universität Berlin, Institut für Hochfrequenz- und Halbleiter-Systemtechnologien: Doctoral thesis. 2017

[142] N.N.: Ormet Circuits Inc.: Ormet Technology Overview. URL http://www.ormetcircuits.com/d/bin-docs/Ormet_Technology_Overview_May_2012.pdf, (Access date: 01.05.2013)

[143] N.N.: Ormet Circuits Inc.: Datasheet Ormet 400. URL www.ormetcircuits.com/d/bin-docs/Ormet_400_Datasheet.pdf, (Access date 01.05.2015)

[144] DIEHM, R.: HPL-Porenfreies Reflow-löten: AiF-Pro INNO II, Förderkennzeichen KA 0251902DA6: HPL-Porenfreies Reflow-löten: AiF-Pro INNO II, Förderkennzeichen KA 0251902DA6. 2009

[145] MOEINI, S. A.; GREVE, H.; MCCLUSKEY, F. P.: Strength and Reliability of High Temperature Transient Liquid Phase Sintered Joints. In: Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT) Vol. 2014 (2014), HITEC, p. 355–363

[146] SYED-KHAJA, A.; FRANKE, J.: Investigations on advanced soldering mechanisms for transient liquid phase soldering (TLPS) in power electronics. In: Electronics System-Integration Technology Conference (ESTC), 2014: 16-18 Sept. 2014, Helsinki. Piscataway, NJ: IEEE, 2014, p. 1–7

[147] SYED-KHAJA, A.; FRANKE, J.: Characterization and Reliability of Paste Based Thin-Film Sn-Cu TLPS Joints for High Temperature Power Electronics. Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2015

[148] SYED-KHAJA, A.; FRANKE, J.: Influential parameters in the development of Transient Liquid Phase Soldering (TLPS) as a new interconnect system for high power lighting applications. In: 2015 IEEE CPMT Symposium Japan (ICSJ): 9-11 Nov. 2015, Kyoto Research Park, Kyoto, Japan. Piscataway, NJ: IEEE, 2015, p. 152–155

[149] SYED-KHAJA, A.; KLEMM, A.; ZERNA, T.; FRANKE, J.: Characterization and Optimization of Sn-Cu TLPS Interconnects for High Temperature Power Electronics through In-Situ-X-Ray Investigations. In: 2016 IEEE 66th Electronic Components and Technology Conference (ECTC): IEEE, 2016, p. 1228–1234

[150] SYED-KHAJA, A.; SCHRAMM, R.; OCHS, R.; FRANKE, J.: Investigations in the Optimization of Power Electronics Packaging through Additive Plasma Technology. In: Procedia CIRP Vol. 37 (2015), p. 59–64

[151] SYED-KHAJA, A.; FRANKE, J.: Process Optimization in Transient Liquid Phase Soldering (TLPS) for an Efficient and Economical Production of High Temperature Power electronics. In: 9th International Conference on Integrated Power Electronics Systems: VDE, 2016

[152] HEUCK, N.; GUTH, K.; THOBEN, M.; MUELLER, A.; OESCHLER, N.; Boewer. L.; SPECKELS, R.; KRASEL, S.; CILIOX, A.: Aging of new Interconnect-Technologies of Power-Modules during Power-Cycling. CIPS 2014; 8th International Conference on Integrated Power Electronics Systems, 2014

[153] HUTTER, M.; WEBER, C.; EHRHARDT, C.; LANG, K. D.: Comparison of different technologies for the die attach of power semiconductor devices conducting active power cycling. In: 9th International Conference on Integrated Power Electronics Systems: VDE, 2016

[154] N.N.: Laser cut stainless steel stencils: Laserjob GmbH. URL http://www.laserjob.com/smd-stencils/stainless-steel-stencil.html (Access date: 30.10.2016)

[155] N.N.: Precision screens: Koennen hightech screens. URL http://www.koenen.de/en/products/precision-screens/the-screen.html, (Access date: 30.10.2016)

[156] CLOUTHIER, R. S.; MELENDEZ, C. A.; JOHNSON, A.: The Complete Solder-Paste-Printing Process-The First in a 2-part Series. In: Surface Mount Technology-Libertyville Vol. 11 (1997), Nr. 5, p. 44–51

[157] LEE, C. C.; KIM, J.: Fundamentals of fluxless soldering technology. In: 2005 10th International Symposium on Advanced Packaging Materials: Processes, properties and interfaces : March 16-18, 2005, Irvine, CA. [New York, N.Y.]: Institute of Electrical and Electronics Engineers, 2005, p. 33–38

[158] MIZUISHI, K.; TOKUDA, M.; FUJITA, Y.: Fluxless and substantially voidless soldering for semiconductor chips. In: 38th Electronics Components Conference 1988., Proceedings: IEEE, 1988, p. 330–334

[159] LEVENSHTEĬN, M. E.; B. I. Shklovskiĭ; M. S. Shur; A. L. Éfros: The relation between the critical exponents of percolation theory. In: Journal of Experimental and Theoretical Physics (JETP) Vol. 42 (1975), Nr. 1, p. 386–392

[160] SONG, C.; WANG, P.; MAKSE, H. A.: A phase diagram for jammed matter. In: Nature Vol. 453 (2008), Nr. 7195, p. 629–632

[161] POWELL, M. J.: Site percolation in randomly packed spheres. In: Physical Review B Vol. 20 (1979), Nr. 10, p. 4194–4198

[162] GALE, W. F.; BUTTS, D. A.: Transient liquid phase bonding. In: Science and Technology of Welding and Joining Vol. 9 (2013), Nr. 4, p. 283–300

[163] TUAH-POKU, I.; DOLLAR, M.; MASSALSKI, T. B.: A study of the transient liquid phase bonding process applied to a Ag/Cu/Ag sandwich joint. In: Metallurgical Transactions A Vol. 19 (1988), Nr. 3, p. 675–686

[164] ABDELFATTAH, M.: An experimental and theoretical study of transient liquid phase bonding of nickel based materials. Ottawa: Library and Archives Canada = Bibliothèque et Archives Canada, 2010

[165] ABDELFATAH, M.; OJO, O. A.: Formation of eutectic-type microconstituent during transient liquid phase bonding of nickel: Influence of process parameters. In: Materials Science and Technology Vol. 25 (2013), Nr. 1, p. 61–67

[166] CHEN, S. J.; TANG, H. J.; JING, X. T.: Transient liquid-phase bonding of T91 steel pipes using amorphous foil. In: Materials Science and Engineering: A Vol. 499 (2009), 1-2, p. 114–117

[167] SCHRAMM, R.: Strukturierte additive Metallisierung durch kaltaktives Atmosphärendruckplasma: Bericht aus dem Lehrstuhl für Fertigungsautomatisierung und Produktionssystematik Prof. Dr.-Ing. Jörg Franke. Bamberg: Meisenbach GmbH Verlag, 2015

[168] SCHRAMM, R.; FRANKE, J.: Electrical Functionalization of Thermoplastic Materials by Cold Active Atmospheric Plasma Technology. In: Proceedings of the 15th Electronics Packaging Technology Conference (EPTC). Singapore, 2013

[169] SCHRAMM, R.; FRANKE, J.: Manufacturing of 3D Mechatronic Systems with Plasma Technology. In: Smart Systems Integration: 8th International Conference & Exhibition on Integration Issues of Miniaturized Systems - MEMS, NEMS, ICs and Electronic Components. Aachen: Apprimus Verlag, 2014, p. 117–123

[170] DIEHM, R.; NOWOTTNICK, M.; PAPE, U.: Reduction of voids in solder joints an alternative to vacuum soldering, Bd. 28. In: Proceedings of IPC APEX EXPO, 2012

[171] KLEMM, A.; JAHNGEN, P.; OPPERMANN, M.; ZERNA, T.: In-situ-X-Ray investigation on pressure release during conventional and diffusion soldering. In: IEEE 15th Electronics Packaging Technology Conference (EPTC), 2013: 11-13 Dec. 2013, Singapore. Piscataway, NJ: IEEE, 2013, p. 821–826

[172] KLEMM, A.; OPPERMANN, M.; ZERNA, T.: In-situ-X-ray investigation on vacuum soldering processes for conventional and diffusion soldering. In: Electronics System-Integration Technology Conference (ESTC), 2014: 16-18 Sept. 2014, Helsinki. Piscataway, NJ: IEEE, 2014, p. 1–6

[173] KLEMM, A.: In-Situ-Charakterisierung von Lötvorgängen für die Leistungselektronik. Dresden, Technische Universität Dresden, Institute for Electronics Packaging Technology (IAVT): Doctoral thesis, 2017

[174] KLEMM, A.; OPPERMANN, M.; ZERNA, T.: Analysis of soldering processes using in-situ X-Ray observations. 2015 European Microelectronics Packaging Conference (EMPC), 2015

[175] LU, M.-H.; HSIEH, K.-C.: Sn-Cu Intermetallic Grain Morphology Related to Sn Layer Thickness. In: Journal of Electronic Materials Vol. 36 (2007), Nr. 11, p. 1448–1454

[176] DENG, X.; PIOTROWSKI, G.; WILLIAMS, J. J.; CHAWLA, N.: Influence of initial morphology and thickness of Cu6Sn5 and Cu3Sn intermetallics on growth and evolution during thermal aging of Sn-Ag solder/Cu joints. In: Journal of Electronic Materials Vol. 32 (2003), Nr. 12, p. 1403–1413

[177] RÖSCH, M.: Potenziale und Strategien zur Optimierung des Schablonendruckprozesses in der Elektronikproduktion. Bamberg: Meisenbach, 2011

[178] SCHRAMM, R.: Plasma in Electronics Production - Today and tomorrow. Plasmatreat International Sales Meeting: Plasmatreat International Sales Meeting. Bielefeld, 19.12.2012

[179] SCHRAMM, R.: Electrical and Mechanical Investigations on Copper Circuit Paths Coated on Fiber-Reinforced Plastics by Atmospheric Plasma Technology. In: Journal of Microelectronics & Electronic Packaging Vol. 12 (2015), Nr. 1, p. 61–66

[180] SCHRAMM, R.; HÖRBER, J.; DOLD, C.; FRANKE, J.: Electrical Functionalization of Thermoplastics by Combining Plasmadust Coating and Aerosol Jet Printing. In: FRANKE, J.; KUHN, T.; BIRKICHT, A.; POJTINGER, A. (ed.): 11th International Congress Molded Interconnect Devices: Scientific Proceedings. Pfaffikon: Trans Tech Publications Ltd, 2014 (Advanced Materials Research, Vol. 1038), p. 43–48

[181] SCHRAMM, R.; REITBERGER, T.; FRANKE, J.: Electrical and Mechanical Investigations on Copper Circuit Paths Coated on Fibre-Reinforced Plastics by Atmospheric Plasma Technology. In: IMAPS (ed.): Journal of Microelectronics and Electronic Packaging, 2015

[182] SCHRAMM, R.; REITBERGER, T.; FRANKE, J.: Electrical Characterization of Fibre-Reinforced Plastics by Atmospheric Plasma Technology. In: International Microelectronics Assembly and Packaging Society (ed.): 47th International Symposium on Microelectronics. San Diego, 2014

[183] DICKINSON, C. F.; HEAL, G. R.: Solid–liquid diffusion controlled rate equations. In: Thermochimica Acta 340-341 (1999), p. 89–103

[184] FICK, A.: On liquid diffusion. In: Journal of Membrane Science Vol. 100 (1995), Nr. 1, p. 33–38

[185] ASSCON Systemtechnik: Multivacuum – The Future of Soldering. URL http://www.asscon.de/e/pages/news/pdf/MULTIVACUUM%20-%20THE%20FUTURE%20OF%20SOLDERING_en.pdf, (Access date: 20.12.2016)

[186] SYED-KHAJA, A.: Project Report Feasibility and Implementation of Diffusion Soldering (TLPS) for High-temperature WBG power devices: Insitute FAPS, Pfarr Stanztechnik GmbH, Powersem GmbH. 2016

[187] HERBERHOLZ, T.: Untersuchungen zu Möglichkeiten und Grenzen des Einsatzes von Zinn-Basislotlegierungen für Hochtemperaturelektronikanwendungen. NOWOTTNICK, M.;WILDE, J.;PAPE, U. (Eds.). Templin: Detert, M, 2015

[188] ROSS, G.; XU, H.; VUORINEN, V.; PAULASTO-KROCKEL, M.: Void formation in Cu-Sn SLID bonding for MEMS. In: Electronics System-Integration Technology Conference (ESTC), 2014: 16-18 Sept. 2014, Helsinki. Piscataway, NJ: IEEE, 2014, p. 1–3

[189] AASMUNDTVEIT, K. E.; LUU, T. T.; WANG, K.; HOIVIK, N.: Void formation in Cu-Sn Solid-Liquid Interdiffusion (SLID) bonding. In: Institute of Electrical and Electronics Engineers (IEEE) (ed.): 2015 European Microelectronics Packaging Conference (EMPC 2015). 1. Ed., 2015

[190] HAMILTON, D. P.; SYED-KHAJA, A.; FRANKE, J.; MAWBY, P.: High temperature thermal cycling reliability of silver sintered and electroplated tin based transient liquid phase joints. In: 9th International Conference on Integrated Power Electronics Systems: VDE, 2016

[191] RAMIREZ, A. G.; HAYES, E. L.: Low melting temperature alloys with magnetic dispersions. Patent Nr. US20110210283 A1

[192] SCHMIDT, W.; KREBS, T.: Adjust the mechanical properties of sintered silver layers using additives. In: 9th International Conference on Integrated Power Electronics Systems: VDE, 2016, p. 1–6

Own publications referring to this work

[P1] SYED-KHAJA, A.; KAESTLE, C.; REINHARDT, A.; FRANKE J.: Optimized thin-film diffusion soldering for power-electronics production. In: IEEE Proceedings of the 36th International Spring Seminar on Electronics Technology, 2013

[P2] SYED-KHAJA, A.; KAESTLE, C.; FRANKE, J.: Reliable packaging technologies for power electronics: Diffusion soldering and heavy copper wire bonding. In: IEEE Proceedings of 3rd International Electric Drives Production Conference (EDPC), 2013

[P3] SYED-KHAJA, A.; FRANKE, J.: Investigations on advanced soldering mechanisms for transient liquid phase soldering (TLPS) in power electronics. In: IEEE Proceedings of the Electronics System-Integration Technology Conference (ESTC), 2014

[P4] SYED-KHAJA, A; FRANKE, J; "Design and Solder Process Optimization in MID Technology for High Power Applications", Advanced Materials Research, Vol. 1038, pp. 107-112, 2014

[P5] SYED-KHAJA, A.; KAESTLE, C.; MUELLER, M.; FRANKE J.: A Comprehensive Study on the Automation Potentials and Complexities of Advanced and Alternative Die-Attach Technologies for Power Electronic Applications. In: Applied Mechanics and Materials, Vol. 794, pp. 320-327, 2015

[P6] SYED-KHAJA, A.; FRANKE, J.: Characterization and Reliability of Paste Based Thin-Film Sn-Cu TLPS Joints for High Temperature Power Electronics. In: Proceedings of PCIM Europe, 2015

[P7] SYED-KHAJA, A.; FRANKE, J.: Influential parameters in the development of Transient Liquid Phase Soldering (TLPS) as a new interconnect system for high power lighting applications. In: Proceedings of IEEE CPMT Symposium Japan (ICSJ), 2015

[P8] SYED-KHAJA, A.; HOERBER, J.; GRUEBER, C.; FRANKE, J.: A novel approach for thin-film Ag-sintering process through Aerosol Jet Printing in power electronics. In: Proceedings of IEEE European Microelectronics Packaging Conference (EMPC), 2015

[P9] SYED-KHAJA, A.; SCHRAMM, R.; OCHS, R.; FRANKE, J.: Investigations in the Optimization of Power Electronics Packaging through Additive Plasma Technology. In: Elsevier Procedia CIRP, Vol. 37, pp.59-64, 2015

[P10] SYED-KHAJA, A.; KLEMM, A..; ZERNA, T.; FRANKE, J.: Characterization and Optimization of Sn-Cu TLPS Interconnects for High Temperature Power Electronics through In-Situ-X-Ray Investigations. In: Proceedings of 2016 IEEE 66th,"Electronic Components and Technology Conference (ECTC), pp.1228-1234, 2016

[P11] SYED-KHAJA, A.; FRANKE, J.: Process Optimization in Transient Liquid Phase Soldering (TLPS) for an Efficient and Economical Production of High Temperature Power electronics. In: ETG-Fachbericht-CIPS 2016, 2016

[P12] SYED-KHAJA, A; STECHER, J.; ESFANDYARI, A.; KREITLEIN. S.; FRANKE, J: Energy Efficient Manufacturing of Power Electronics Substrates through Selective Laser Melting Technology. In: Applied Mechanics and Materials, Vol. 856, pp. 188-194, 2017

[P13] KAESTLE, C.; SYED-KHAJA, A.; REINHARDT, A.; FRANKE J.: Investigations on ultrasonic copper wire wedge bonding for power electronics. In: IEEE Proceedings of the 36th International Spring Seminar on Electronics Technology, 2013

[P14] ESFANDYARI, A.; SYED-KHAJA, A.; TALLAL, J.; FRANKE, J.; Energy Efficiency Investigation on High-Pressure Convection Reflow Soldering in Electronics Production, Applied Mechanics & Materials, Vol.655, 2014

[P15] ESFANDYARI, A.; SYED-KHAJA, A.; LANDSKRONE, T.; FRANKE, J.: An Exergy-Based Analysis of Temperature Profiles for an Over-Pressure Reflow Oven Technology. In: ASME 2015 International Mechanical Engineering Congress and Exposition, 2015

[P16] ESFANDYARI, A.; SYED-KHAJA, A.; HORVATH, M.; FRANKE, J.: Energy Efficiency Analysis of Vapor Phase Soldering Technology through Exergy-Based Metric. In: Applied Mechanics and Materials, Vol. 805, pp. 196-204, 2015

[P17] HAMILTON, D. P; SYED-KHAJA, A.; FRANKE, J; MAWBY, P.; ,High temperature thermal cycling reliability of silver sintered and electroplated tin based transient liquid phase joints. In: ETG-Fachbericht-CIPS 2016, 2016

[P18] ESFANDYARI, A.; SYED-KHAJA, A.; SAETTLER, D.; FRANKE, J.: A Lean-Based Key Performance Analysis for a Resource Efficient Soldering Oven in Electronics Production. In: Applied Mechanics and Materials, Vol. 856, pp. 91-98, 2017.

Publications on the other topics

[P19] SYED-KHAJA, A.; SCHWARZ, D.; FRANKE, J.: Advanced substrate and packaging concepts for compact system integration with additive manufacturing technologies for high temperature applications. In: 2015 IEEE CPMT Symposium Japan (ICSJ), 2015

[P20] SYED-KHAJA, A.; KAESTLE, C.; FRANKE, J.: Feasibility Studies on Selective Laser Melting of Copper Powders for the Development of High-temperature Circuit Carriers. In: International Microelectronics Assembly and Packaging Society Symposium, 2016

[P21] SYED-KHAJA, A.; WALAWSKI D.; STOLL, T.; FRANKE, J.: Is selective laser melting (SLM) an alternative for high-temperature mechatronic integrated devices? Methodology, hurdles and prospects. In: IEEE Proceedings of 12th International Congress Molded Interconnect Devices (MID), 2016

[P22] SYED-KHAJA, A.; FRANKE, J.: Selective Laser Melting for Additive Manufacturing of High-temperature Ceramic Circuit Carriers. In: 2016 IEEE 66th Electronic Components and Technology Conference (ECTC), 2016

[P23] SYED-KHAJA, A.; PEREZ, P. FRANKE, J.: Production and characterization of high-temperature substrates through selective laser melting (SLM) for power electronics. In: 2016 Proceedings of IEEE CPMT Symposium Japan (ICSJ), 2016

[P24] SYED-KHAJA, A.; STOLL, T.; FRANKE, J.: Investigations in selective laser melting as manufacturing technology for the production of high-temperature mechatronic integrated devices. In: 2016 Proceedings of 11th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), 2016

[P25] SYED-KHAJA, A.; STECHER, J.; ESFANDYARI, A.; KREITLEIN, S.; FRANKE, J.: Energy Efficient Manufacturing of Power Electronics Substrates through Selective Laser Melting Technology. In: Applied Mechanics and Materials, Vol.856, pp.188-194, 2017

[P26] SYED-KHAJA, A.; FREIRE, A.P.; KAESTLE, C.; FRANKE, J.: Feasibility Investigations on Selective Laser Melting for the Development of Microchannel Cooling in Power Electronics. In: 2017 IEEE 67th Electronic Components and Technology Conference (ECTC), 2017

[P27] KREITLEIN, S.; EDER, N.; SYED-KHAJA, A.; FRANKE, J.: Comprehensive Assessment of Energy Efficiency within the Production Process. In: World Academy of Science, Engineering and Technology, International Journal of Mechanical, Aerospace, Industrial, Mechatronic and Manufacturing Engineering", Vol.9, pp-1343-1350, 2015

[P28] KAESTLE, C.; SYED-KHAJA, A.; FRANKE J.: Investigations on the Wire Bonding Capability on Selective Laser Melted Structures. In: 2016 International Microelec-tronics Assembly and Packaging Society Symposium on Microelectronics, 2016.

Student' theses referring to this work

The preparation of assemblies, evaluations, research and investigations took place through the task description and under the technical guidance of the author with the support of the following student works:

[S1] STRAUMEIER, C.; SYED-KHAJA, A.; FRANKE, J.: Construction and Testing of Reliable Interconnection Technology for Power Electronics: Diffusion Soldering. Bachelor thesis. Nuremberg, 2013.

[S2] MICHELS, T.; SYED-KHAJA, A.; KAESTLE, C.; FRANKE, J.: Aufbau und Prüfung zuverlässiger Verbindungstechnologien für die Leistungselektronik: Diffusionslöten und Kupfer-Dickdrahtbonden. Master thesis. Nuremberg, 2013.

[S3] OCHS, R.; SYED-KHAJA, A.; SCHRAMM, R.; FRANKE, J.: Konzeption und Evaluierung einer Prozessstrategie zur Herstellung zuverlässiger Diffusionslöt-verbindungen in der Leistungselektronik durch den Einsatz der Plasmadust®-Technologie. Diploma thesis. Nuremberg, 2014.

[S4] SCHNIEDERS, H.; SYED-KHAJA, A.; FRANKE, J.: Evaluation von Prozessparametern für einen zuverlässigen Überdruck-Reflowlötprozess in der Leistungselektronik. Bachelor thesis. Nuremberg, 2014.

[S5] DEURINGER, M.; SYED-KHAJA, A.; FRANKE, J.: Untersuchungen zum Einsatz fortschrittlicher Reflow-Lötverfahren für die SMD basierten Technologien. Bachelor thesis. Nuremberg, 2014.

[S6] WOLF, P.; SYED-KHAJA, A.; FRANKE, J.: Thermische- und strukturelle Charakterisierung von Hochtemperatur Die-Attach-Technologien in der Leistungselektronik. Bachelor thesis. Nuremberg, 2014.

[S7] GRÜBER, C.; SYED-KHAJA, A.; HOERBER, J.; FRANKE, J.: Umsetzung und Prüfung von Ag-Sintertechnologie zur zuverlässigen Verbindungen in der Leistungselektronik. Diploma thesis. Nuremberg, 2014.

[S8] BRANDES, N.; SYED-KHAJA, A.; FRANKE, J.: Evaluation von Prozessparametern für einen zuverlässigen Überdruck-Reflowlötprozess in der Leistungselektronik. Bachelor thesis. Nuremberg, 2015.

[S9] HOFFMAN, D.; SYED-KHAJA, A.; FRANKE, J.: Untersuchung von thermo-mechanisch belasteten Lötstellen mittels der Finiten-Elemente-Methode (FEM) zur Bewertung ihrer Zuverlässigkeit. Bachelor thesis. Nuremberg, 2015.

[S10] HERINGLEHNER, M.; SYED-KHAJA, A.; FRANKE, J.: Evaluation von Prozessparametern für einen zuverlässigen Vakuum-Dampfphasen-Reflowlötprozess in der Leistungselektronik. Bachelor thesis. Nuremberg, 2015.

[S11] HOFMANN, B.; SYED-KHAJA, A.; FRANKE, J.: Aufbau und Prüfung zuverlässiger Verbindungstechnologie für die Leistungselektronik: Diffusionslöten. Bachelor thesis. Nuremberg, 2015.

[S12] CHAKI, C.; SYED-KHAJA, A.; FRANKE, J.: Modelling and Simulation of Intermetallic Compound Formation in Diffusion Soldering Interconnections for Power Electronics Applications. Master thesis. Nuremberg, 2015.

[S13] DAESCHLE, S.; SYED-KHAJA, A.; FRANKE, J.: Erfassung und Bewertung aktueller Trends in der Leistungselekt-ronik. Project work. Nuremberg, 2015.

[S14] JARY, C.; SYED-KHAJA, A.; FRANKE, J.: Investigations on the Inter-Metallic Phase Formation in Cu-Sn Bimetallic Systems for Power Electronics Applications. Bachelor thesis. Nuremberg, 2015.

[S15] KELS, C.; SYED-KHAJA, A.; FRANKE, J.: Evaluation of silver adhesive printing process for automotive applications. Master thesis. Nuremberg, 2015.

Supervised student works in other subject areas[1]

[S16] SENNEFELDER, S.; SYED-KHAJA, A.; FRANKE, J.: Market evaluation and technology analysis of printed and organic electronics. Project work. Nuremberg, 2013.

[S17] SCHWARZ, D.; SYED-KHAJA, A.; FRANKE, J.: Qualifizierung und Quantifizierung des selektiven Laser-schmelzprozesses zur Herstellung von Keramik Schaltungsträgern in der Leistungselektronik. Master thesis. Nuremberg, 2015.

[S18] KOCH, O.; SYED-KHAJA, A.; FRANKE, J.: Erfassung und Bewertung aktueller Trends in der Leistungselektronik und Aufbau einer Datenbank. Project work. Nuremberg, 2015.

[S19] FRANK, S.; SYED-KHAJA, A.; FRANKE, J.: Trends in der Additiven Fertigung – Eine Literaturrecherche und Einsatzmöglichkeiten zum Laserstrahlschmelz-Verfahren in der Leistungselektronik. Project work. Nuremberg, 2015.

[S20] PATINO PEREZ, P.; SYED-KHAJA, A.; FRANKE, J.: Evaluierung der additiv hergestellten SLM-Leiterbahnen mittels Stromtragfähigkeitsuntersuchungen. Bachelor thesis. Nuremberg, 2015.

[S21] STECHER, J.; SYED-KHAJA, A.; FRANKE, J.: Analyse des Energie- und Rohstoffverbrauchs beim Herstellen von Keramikschaltungsträgern mittels Selective Laser Melting. Bachelor thesis. Nuremberg, 2015.

[S22] STÖCKLEIN, J.; SYED-KHAJA, A.; FRANKE, J.: Nachforschungen an thermisch nachbehandelten mittels selektivem Laserschmelzen gefertigten Strukturen. Bachelor thesis. Nuremberg, 2016.

[S23] WALAWSKI, D.; SYED-KHAJA, A.; FRANKE, J.: Machbarkeitsprüfung zur Minimierung von auf Keramiksubstrat hergestellten Leiterbahnen aus Kupfer mittels Selektiv-Laserschmelzen. Bachelor thesis. Nuremberg, 2015.

[S24] FREIRE JESUS, A.; SYED-KHAJA, A.; FRANKE, J: Conceptualization and Feasibility Investigations on the Development of Advanced Thermal Management through SLM Technology for Power Electronics. Master thesis. Nuremberg, 2016.

[S25] STOLL, T.; SYED-KHAJA, A.; FRANKE, J.: Einflüsse der Oberflächeneigenschaften von Keramik in der selektiven Laserschmelzen von Kupferpulver für die additive Fertigung von leistungselektronischen Substraten. Master thesis. Nuremberg, 2016.

[S26] GUTMANN, S.; SYED-KHAJA, A.; FRANKE, J.: Market analysis and feasibility report on the additive manufacturing techniques for power electronics applications. Project work. Nuremberg, 2017.

[S27] GUTMANN, S.; SYED-KHAJA, A.; FRANKE, J.: Untersuchungen zum Einsatz fortschrittlicher Verbindungstechnologien für SLM-generierte keramische Schaltungsträger. Master thesis. Nuremberg, 2016.

[S28] KIES, E.; SYED-KHAJA, A.; FRANKE, J.: Eignung des selektiven Laserschmelzens zur Herstellung von additiv aufgebauten Leistungselektronik Schaltungsträgern, Prozessvergleich und praktische Erprobung. Bachelor thesis. Nuremberg, 2016.

[S29] TISCHER, E.; SYED-KHAJA, A.; FRANKE, J.: Zuverlässigkeitsuntersuchungen von ausgewählten Verbindungs-technologien auf SLM-Strukturen. Project work. Nuremberg, 2016.

[S30] STÖCKLEIN, J.; SYED-KHAJA, A.; FRANKE, J.: Nachforschungen an thermisch nachbehandelten mittels selektivem Laserschmelzen gefertigten Kupfer- und Bronzestrukturen. Project work. Nuremberg, 2016.

---

[1] The 2nd (3rd) author names the supervisor; the last author is head of the institute

Reihenübersicht

Koordination der Reihe (Stand 12/2018):
Geschäftsstelle Maschinenbau, Dr.-Ing. Oliver Kreis, www.mb.fau.de/diss/

Im Rahmen der Reihe sind bisher die nachfolgenden Bände erschienen.

Band 1 – 52
Fertigungstechnik – Erlangen
ISSN 1431-6226
Carl Hanser Verlag, München

Band 53 – 307
Fertigungstechnik – Erlangen
ISSN 1431-6226
Meisenbach Verlag, Bamberg

ab Band 308
FAU Studien aus dem Maschinenbau
ISSN 2625-9974
FAU University Press, Erlangen

Die Zugehörigkeit zu den jeweiligen Lehrstühlen ist wie folgt gekennzeichnet:

Lehrstühle:

FAPS	Lehrstuhl für Fertigungsautomatisierung und Produktionssystematik
LFT	Lehrstuhl für Fertigungstechnologie
LPT	Lehrstuhl für Photonische Technologien

Band 1: Andreas Hemberger
Innovationspotentiale in der rechnerintegrierten Produktion durch wissensbasierte Systeme
FAPS, 208 Seiten, 107 Bilder. 1988.
ISBN 3-446-15234-2.

Band 2: Detlef Classe
Beitrag zur Steigerung der Flexibilität automatisierter Montagesysteme durch Sensorintegration und erweiterte Steuerungskonzepte
FAPS, 194 Seiten, 70 Bilder. 1988.
ISBN 3-446-15529-5.

Band 3: Friedrich-Wilhelm Nolting
Projektierung von Montagesystemen
FAPS, 201 Seiten, 107 Bilder, 1 Tab. 1989.
ISBN 3-446-15541-4.

Band 4: Karsten Schlüter
Nutzungsgradsteigerung von Montagesystemen durch den Einsatz der Simulationstechnik
FAPS, 177 Seiten, 97 Bilder. 1989.
ISBN 3-446-15542-2.

Band 5: Shir-Kuan Lin
Aufbau von Modellen zur Lageregelung von Industrierobotern
FAPS, 168 Seiten, 46 Bilder. 1989.
ISBN 3-446-15546-5.

Band 6: Rudolf Nuss
Untersuchungen zur Bearbeitungsqualität im Fertigungssystem Laserstrahlschneiden
LFT, 206 Seiten, 115 Bilder, 6 Tab. 1989.
ISBN 3-446-15783-2.

Band 7: Wolfgang Scholz
Modell zur datenbankgestützten Planung automatisierter Montageanlagen
FAPS, 194 Seiten, 89 Bilder. 1989.
ISBN 3-446-15825-1.

Band 8: Hans-Jürgen Wißmeier
Beitrag zur Beurteilung des Bruchverhaltens von Hartmetall-Fließpreßmatrizen
LFT, 179 Seiten, 99 Bilder, 9 Tab. 1989.
ISBN 3-446-15921-5.

Band 9: Rainer Eisele
Konzeption und Wirtschaftlichkeit von Planungssystemen in der Produktion
FAPS, 183 Seiten, 86 Bilder. 1990.
ISBN 3-446-16107-4.

Band 10: Rolf Pfeiffer
Technologisch orientierte Montageplanung am Beispiel der Schraubtechnik
FAPS, 216 Seiten, 102 Bilder, 16 Tab. 1990.
ISBN 3-446-16161-9.

Band 11: Herbert Fischer
Verteilte Planungssysteme zur Flexibilitätssteigerung der rechnerintegrierten Teilefertigung
FAPS, 201 Seiten, 82 Bilder. 1990.
ISBN 3-446-16105-8.

Band 12: Gerhard Kleineidam
CAD/CAP: Rechnergestützte Montagefeinplanung
FAPS, 203 Seiten, 107 Bilder. 1990.
ISBN 3-446-16112-0.

Band 13: Frank Vollertsen
Pulvermetallurgische Verarbeitung eines übereutektoiden verschleißfesten Stahls
LFT, XIII u. 217 Seiten, 67 Bilder, 34 Tab. 1990. ISBN 3-446-16133-3.

Band 14: Stephan Biermann
Untersuchungen zur Anlagen- und Prozeßdiagnostik für das Schneiden mit CO_2-Hochleistungslasern
LFT, VIII u. 170 Seiten, 93 Bilder, 4 Tab. 1991. ISBN 3-446-16269-0.

Band 15: Uwe Geißler
Material- und Datenfluß in einer flexiblen Blechbearbeitungszelle
LFT, 124 Seiten, 41 Bilder, 7 Tab. 1991.
ISBN 3-446-16358-1.

Band 16: Frank Oswald Hake
Entwicklung eines rechnergestützten Diagnosesystems für automatisierte Montagezellen
FAPS, XIV u. 166 Seiten, 77 Bilder. 1991.
ISBN 3-446-16428-6.

Band 17: Herbert Reichel
Optimierung der Werkzeugbereitstellung durch rechnergestützte Arbeitsfolgenbestimmung
FAPS, 198 Seiten, 73 Bilder, 2 Tab. 1991.
ISBN 3-446-16453-7.

Band 18: Josef Scheller
Modellierung und Einsatz von Softwaresystemen für rechnergeführte Montagezellen
FAPS, 198 Seiten, 65 Bilder. 1991.
ISBN 3-446-16454-5.

Band 19: Arnold vom Ende
Untersuchungen zum Biegeumforme mit elastischer Matrize
LFT, 166 Seiten, 55 Bilder, 13 Tab. 1991.
ISBN 3-446-16493-6.

Band 20: Joachim Schmid
Beitrag zum automatisierten Bearbeiten von Keramikguß mit Industrierobotern
FAPS, XIV u. 176 Seiten, 111 Bilder, 6 Tab. 1991. ISBN 3-446-16560-6.

Band 21: Egon Sommer
Multiprozessorsteuerung für kooperierende Industrieroboter in Montagezellen
FAPS, 188 Seiten, 102 Bilder. 1991.
ISBN 3-446-17062-6.

Band 22: Georg Geyer
Entwicklung problemspezifischer Verfahrensketten in der Montage
FAPS, 192 Seiten, 112 Bilder. 1991.
ISBN 3-446-16552-5.

Band 23: Rainer Flohr
Beitrag zur optimalen Verbindungstechnik in der Oberflächenmontage (SMT)
FAPS, 186 Seiten, 79 Bilder. 1991.
ISBN 3-446-16568-1.

Band 24: Alfons Rief
Untersuchungen zur Verfahrensfolge Laserstrahlschneiden und -schweißen in der Rohkarosseriefertigung
LFT, VI u. 145 Seiten, 58 Bilder, 5 Tab. 1991. ISBN 3-446-16593-2.

Band 25: Christoph Thim
Rechnerunterstützte Optimierung von Materialflußstrukturen in der Elektronikmontage durch Simulation
FAPS, 188 Seiten, 74 Bilder. 1992.
ISBN 3-446-17118-5.

Band 26: Roland Müller
CO_2 -Laserstrahlschneiden von kurzglasverstärkten Verbundwerkstoffen
LFT, 141 Seiten, 107 Bilder, 4 Tab. 1992.
ISBN 3-446-17104-5.

Band 27: Günther Schäfer
Integrierte Informationsverarbeitung bei der Montageplanung
FAPS, 195 Seiten, 76 Bilder. 1992.
ISBN 3-446-17117-7.

Band 28: Martin Hoffmann
Entwicklung einer CAD/CAM-Prozeßkette für die Herstellung von Blechbiegeteilen
LFT, 149 Seiten, 89 Bilder. 1992.
ISBN 3-446-17154-1.

Band 29: Peter Hoffmann
Verfahrensfolge Laserstrahlschneiden und –schweißen: Prozeßführung und Systemtechnik in der 3D-Laserstrahlbearbeitung von Blechformteilen
LFT, 186 Seiten, 92 Bilder, 10 Tab. 1992.
ISBN 3-446-17153-3.

Band 30: Olaf Schrödel
Flexible Werkstattsteuerung mit objektorientierten Softwarestrukturen
FAPS, 180 Seiten, 84 Bilder. 1992.
ISBN 3-446-17242-4.

Band 31: Hubert Reinisch
Planungs- und Steuerungswerkzeuge zur impliziten Geräteprogrammierung in Roboterzellen
FAPS, XI u. 212 Seiten, 112 Bilder. 1992.
ISBN 3-446-17380-3.

Band 32: Brigitte Bärnreuther
Ein Beitrag zur Bewertung des Kommunikationsverhaltens von Automatisierungsgeräten in flexiblen Produktionszellen
FAPS, XI u. 179 Seiten, 71 Bilder. 1992.
ISBN 3-446-17451-6.

Band 33: Joachim Hutfless
Laserstrahlregelung und Optikdiagnostik in der Strahlführung einer CO_2-Hochleistungslaseranlage
LFT, 175 Seiten, 70 Bilder, 17 Tab. 1993.
ISBN 3-446-17532-6.

Band 34: Uwe Günzel
Entwicklung und Einsatz eines Simulationsverfahrens für operative und strategische Probleme der Produktionsplanung und –steuerung
FAPS, XIV u. 170 Seiten, 66 Bilder, 5 Tab. 1993. ISBN 3-446-17604-7.

Band 35: Bertram Ehmann
Operatives Fertigungscontrolling durch Optimierung auftragsbezogener Bearbeitungsabläufe in der Elektronikfertigung
FAPS, XV u. 167 Seiten, 114 Bilder. 1993.
ISBN 3-446-17658-6.

Band 36: Harald Kolléra
Entwicklung eines benutzerorientierten Werkstattprogrammiersystems für das Laserstrahlschneiden
LFT, 129 Seiten, 66 Bilder, 1 Tab. 1993.
ISBN 3-446-17719-1.

Band 37: Stephanie Abels
Modellierung und Optimierung von Montageanlagen in einem integrierten Simulationssystem
FAPS, 188 Seiten, 88 Bilder. 1993.
ISBN 3-446-17731-0.

Band 38: Robert Schmidt-Hebbel
Laserstrahlbohren durchflußbestimmender Durchgangslöcher
LFT, 145 Seiten, 63 Bilder, 11 Tab. 1993.
ISBN 3-446-17778-7.

Band 39: Norbert Lutz
Oberflächenfeinbearbeitung keramischer Werkstoffe mit XeCl-Excimerlaserstrahlung
LFT, 187 Seiten, 98 Bilder, 29 Tab. 1994.
ISBN 3-446-17970-4.

Band 40: Konrad Grampp
Rechnerunterstützung bei Test und Schulung an Steuerungssoftware von SMD-Bestücklinien
FAPS, 178 Seiten, 88 Bilder. 1995.
ISBN 3-446-18173-3.

Band 41: Martin Koch
Wissensbasierte Unterstützung der Angebotsbearbeitung in der Investitionsgüterindustrie
FAPS, 169 Seiten, 68 Bilder. 1995.
ISBN 3-446-18174-1.

Band 42: Armin Gropp
Anlagen- und Prozeßdiagnostik beim Schneiden mit einem gepulsten Nd:YAG-Laser
LFT, 160 Seiten, 88 Bilder, 7 Tab. 1995.
ISBN 3-446-18241-1.

Band 43: Werner Heckel
Optische 3D-Konturerfassung und on-line Biegewinkelmessung mit dem Lichtschnittverfahren
LFT, 149 Seiten, 43 Bilder, 11 Tab. 1995.
ISBN 3-446-18243-8.

Band 44: Armin Rothhaupt
Modulares Planungssystem zur Optimierung der Elektronikfertigung
FAPS, 180 Seiten, 101 Bilder. 1995.
ISBN 3-446-18307-8.

Band 45: Bernd Zöllner
Adaptive Diagnose in der Elektronikproduktion
FAPS, 195 Seiten, 74 Bilder, 3 Tab. 1995.
ISBN 3-446-18308-6.

Band 46: Bodo Vormann
Beitrag zur automatisierten Handhabungsplanung komplexer Blechbiegeteile
LFT, 126 Seiten, 89 Bilder, 3 Tab. 1995.
ISBN 3-446-18345-0.

Band 47: Peter Schnepf
Zielkostenorientierte Montageplanung
FAPS, 144 Seiten, 75 Bilder. 1995.
ISBN 3-446-18397-3.

Band 48: Rainer Klotzbücher
Konzept zur rechnerintegrierten Materialversorgung in flexiblen Fertigungssystemen
FAPS, 156 Seiten, 62 Bilder. 1995.
ISBN 3-446-18412-0.

Band 49: Wolfgang Greska
Wissensbasierte Analyse und Klassifizierung von Blechteilen
LFT, 144 Seiten, 96 Bilder. 1995.
ISBN 3-446-18462-7.

Band 50: Jörg Franke
Integrierte Entwicklung neuer Produkt- und Produktionstechnologien für räumliche spritzgegossene Schaltungsträger (3-D MID)
FAPS, 196 Seiten, 86 Bilder, 4 Tab. 1995.
ISBN 3-446-18448-1.

Band 51: Franz-Josef Zeller
Sensorplanung und schnelle Sensorregelung für Industrieroboter
FAPS, 190 Seiten, 102 Bilder, 9 Tab. 1995.
ISBN 3-446-18601-8.

Band 52: Michael Solvie
Zeitbehandlung und Multimedia-Unterstützung in Feldkommunikationssystemen
FAPS, 200 Seiten, 87 Bilder, 35 Tab. 1996.
ISBN 3-446-18607-7.

Band 53: Robert Hopperdietzel
Reengineering in der Elektro- und Elektronikindustrie
FAPS, 180 Seiten, 109 Bilder, 1 Tab. 1996.
ISBN 3-87525-070-2.

Band 54: Thomas Rebhahn
Beitrag zur Mikromaterialbearbeitung mit Excimerlasern - Systemkomponenten und Verfahrensoptimierungen
LFT, 148 Seiten, 61 Bilder, 10 Tab. 1996.
ISBN 3-87525-075-3.

Band 55: Henning Hanebuth
Laserstrahlhartlöten mit Zweistrahltechnik
LFT, 157 Seiten, 58 Bilder, 11 Tab. 1996.
ISBN 3-87525-074-5.

Band 56: Uwe Schönherr
Steuerung und Sensordatenintegration für flexible Fertigungszellen mit kooperierenden Robotern
FAPS, 188 Seiten, 116 Bilder, 3 Tab. 1996.
ISBN 3-87525-076-1.

Band 57: Stefan Holzer
Berührungslose Formgebung mit Laserstrahlung
LFT, 162 Seiten, 69 Bilder, 11 Tab. 1996.
ISBN 3-87525-079-6.

Band 58: Markus Schultz
Fertigungsqualität beim 3D-Laserstrahlschweißen von Blechformteilen
LFT, 165 Seiten, 88 Bilder, 9 Tab. 1997.
ISBN 3-87525-080-X.

Band 59: Thomas Krebs
Integration elektromechanischer CA-Anwendungen über einem STEP-Produktmodell
FAPS, 198 Seiten, 58 Bilder, 8 Tab. 1997.
ISBN 3-87525-081-8.

Band 60: Jürgen Sturm
Prozeßintegrierte Qualitätssicherung in der Elektronikproduktion
FAPS, 167 Seiten, 112 Bilder, 5 Tab. 1997.
ISBN 3-87525-082-6.

Band 61: Andreas Brand
Prozesse und Systeme zur Bestückung räumlicher elektronischer Baugruppen (3D-MID)
FAPS, 182 Seiten, 100 Bilder. 1997.
ISBN 3-87525-087-7.

Band 62: Michael Kauf
Regelung der Laserstrahlleistung und der Fokusparameter einer CO_2-Hochleistungslaseranlage
LFT, 140 Seiten, 70 Bilder, 5 Tab. 1997.
ISBN 3-87525-083-4.

Band 63: Peter Steinwasser
Modulares Informationsmanagement in der integrierten Produkt- und Prozeßplanung
FAPS, 190 Seiten, 87 Bilder. 1997.
ISBN 3-87525-084-2.

Band 64: Georg Liedl
Integriertes Automatisierungskonzept für den flexiblen Materialfluß in der Elektronikproduktion
FAPS, 196 Seiten, 96 Bilder, 3 Tab. 1997.
ISBN 3-87525-086-9.

Band 65: Andreas Otto
Transiente Prozesse beim Laserstrahlschweißen
LFT, 132 Seiten, 62 Bilder, 1 Tab. 1997.
ISBN 3-87525-089-3.

Band 66: Wolfgang Blöchl
Erweiterte Informationsbereitstellung an offenen CNC-Steuerungen zur Prozeß- und Programmoptimierung
FAPS, 168 Seiten, 96 Bilder. 1997.
ISBN 3-87525-091-5.

Band 67: Klaus-Uwe Wolf
Verbesserte Prozeßführung und Prozeßplanung zur Leistungs- und Qualitätssteigerung beim Spulenwickeln
FAPS, 186 Seiten, 125 Bilder. 1997.
ISBN 3-87525-092-3.

Band 68: Frank Backes
Technologieorientierte Bahnplanung für die 3D-Laserstrahlbearbeitung
LFT, 138 Seiten, 71 Bilder, 2 Tab. 1997.
ISBN 3-87525-093-1.

Band 69: Jürgen Kraus
Laserstrahlumformen von Profilen
LFT, 137 Seiten, 72 Bilder, 8 Tab. 1997.
ISBN 3-87525-094-X.

Band 70: Norbert Neubauer
Adaptive Strahlführungen für CO_2-Laseranlagen
LFT, 120 Seiten, 50 Bilder, 3 Tab. 1997.
ISBN 3-87525-095-8.

Band 71: Michael Steber
Prozeßoptimierter Betrieb flexibler Schraubstationen in der automatisierten Montage
FAPS, 168 Seiten, 78 Bilder, 3 Tab. 1997.
ISBN 3-87525-096-6.

Band 72: Markus Pfestorf
Funktionale 3D-Oberflächenkenngrößen in der Umformtechnik
LFT, 162 Seiten, 84 Bilder, 15 Tab. 1997.
ISBN 3-87525-097-4.

Band 73: Volker Franke
Integrierte Planung und Konstruktion von Werkzeugen für die Biegebearbeitung
LFT, 143 Seiten, 81 Bilder. 1998.
ISBN 3-87525-098-2.

Band 74: Herbert Scheller
Automatisierte Demontagesysteme und recyclinggerechte Produktgestaltung elektronischer Baugruppen
FAPS, 184 Seiten, 104 Bilder, 17 Tab. 1998.
ISBN 3-87525-099-0.

Band 75: Arthur Meßner
Kaltmassivumformung metallischer Kleinstteile - Werkstoffverhalten, Wirkflächenreibung, Prozeßauslegung
LFT, 164 Seiten, 92 Bilder, 14 Tab. 1998.
ISBN 3-87525-100-8.

Band 76: Mathias Glasmacher
Prozeß- und Systemtechnik zum Laserstrahl-Mikroschweißen
LFT, 184 Seiten, 104 Bilder, 12 Tab. 1998.
ISBN 3-87525-101-6.

Band 77: Michael Schwind
Zerstörungsfreie Ermittlung mechanischer Eigenschaften von Feinblechen mit dem Wirbelstromverfahren
LFT, 124 Seiten, 68 Bilder, 8 Tab. 1998.
ISBN 3-87525-102-4.

Band 78: Manfred Gerhard
Qualitätssteigerung in der Elektronikproduktion durch Optimierung der Prozeßführung beim Löten komplexer Baugruppen
FAPS, 179 Seiten, 113 Bilder, 7 Tab. 1998.
ISBN 3-87525-103-2.

Band 79: Elke Rauh
Methodische Einbindung der Simulation in die betrieblichen Planungs- und Entscheidungsabläufe
FAPS, 192 Seiten, 114 Bilder, 4 Tab. 1998.
ISBN 3-87525-104-0.

Band 80: Sorin Niederkorn
Meßeinrichtung zur Untersuchung der Wirkflächenreibung bei umformtechnischen Prozessen
LFT, 99 Seiten, 46 Bilder, 6 Tab. 1998.
ISBN 3-87525-105-9.

Band 81: Stefan Schuberth
Regelung der Fokuslage beim Schweißen mit CO2-Hochleistungslasern unter Einsatz von adaptiven Optiken
LFT, 140 Seiten, 64 Bilder, 3 Tab. 1998.
ISBN 3-87525-106-7.

Band 82: Armando Walter Colombo
Development and Implementation of Hierarchical Control Structures of Flexible Production Systems Using High Level Petri Nets
FAPS, 216 Seiten, 86 Bilder. 1998.
ISBN 3-87525-109-1.

Band 83: Otto Meedt
Effizienzsteigerung bei Demontage und Recycling durch flexible Demontagetechnologien und optimierte Produktgestaltung
FAPS, 186 Seiten, 103 Bilder. 1998.
ISBN 3-87525-108-3.

Band 84: Knuth Götz
Modelle und effiziente Modellbildung zur Qualitätssicherung in der Elektronikproduktion
FAPS, 212 Seiten, 129 Bilder, 24 Tab. 1998.
ISBN 3-87525-112-1.

Band 85: Ralf Luchs
Einsatzmöglichkeiten leitender Klebstoffe zur zuverlässigen Kontaktierung elektronischer Bauelemente in der SMT
FAPS, 176 Seiten, 126 Bilder, 30 Tab. 1998.
ISBN 3-87525-113-7.

Band 86: Frank Pöhlau
Entscheidungsgrundlagen zur Einführung räumlicher spritzgegossener Schaltungsträger (3-D MID)
FAPS, 144 Seiten, 99 Bilder. 1999.
ISBN 3-87525-114-8.

Band 87: Roland T. A. Kals
Fundamentals on the miniaturization of sheet metal working processes
LFT, 128 Seiten, 58 Bilder, 11 Tab. 1999.
ISBN 3-87525-115-6.

Band 88: Gerhard Luhn
Implizites Wissen und technisches Handeln am Beispiel der Elektronikproduktion
FAPS, 252 Seiten, 61 Bilder, 1 Tab. 1999.
ISBN 3-87525-116-4.

Band 89: Axel Sprenger
Adaptives Streckbiegen von Aluminium-Strangpreßprofilen
LFT, 114 Seiten, 63 Bilder, 4 Tab. 1999.
ISBN 3-87525-117-2.

Band 90: Hans-Jörg Pucher
Untersuchungen zur Prozeßfolge Umformen, Bestücken und Laserstrahllöten von Mikrokontakten
LFT, 158 Seiten, 69 Bilder, 9 Tab. 1999.
ISBN 3-87525-119-9.

Band 91: Horst Arnet
Profilbiegen mit kinematischer Gestalterzeugung
LFT, 128 Seiten, 67 Bilder, 7 Tab. 1999.
ISBN 3-87525-120-2.

Band 92: Doris Schubart
Prozeßmodellierung und Technologieentwicklung beim Abtragen mit CO_2-Laserstrahlung
LFT, 133 Seiten, 57 Bilder, 13 Tab. 1999.
ISBN 3-87525-122-9.

Band 93: Adrianus L. P. Coremans
Laserstrahlsintern von Metallpulver - Prozeßmodellierung, Systemtechnik, Eigenschaften laserstrahlgesinterter Metallkörper
LFT, 184 Seiten, 108 Bilder, 12 Tab. 1999.
ISBN 3-87525-124-5.

Band 94: Hans-Martin Biehler
Optimierungskonzepte für Qualitätsdatenverarbeitung und Informationsbereitstellung in der Elektronikfertigung
FAPS, 194 Seiten, 105 Bilder. 1999.
ISBN 3-87525-126-1.

Band 95: Wolfgang Becker
Oberflächenausbildung und tribologische Eigenschaften excimerlaserstrahlbearbeiteter Hochleistungskeramiken
LFT, 175 Seiten, 71 Bilder, 3 Tab. 1999.
ISBN 3-87525-127-X.

Band 96: Philipp Hein
Innenhochdruck-Umformen von Blechpaaren: Modellierung, Prozeßauslegung und Prozeßführung
LFT, 129 Seiten, 57 Bilder, 7 Tab. 1999.
ISBN 3-87525-128-8.

Band 97: Gunter Beitinger
Herstellungs- und Prüfverfahren für thermoplastische Schaltungsträger
FAPS, 169 Seiten, 92 Bilder, 20 Tab. 1999.
ISBN 3-87525-129-6.

Band 98: Jürgen Knoblach
Beitrag zur rechnerunterstützten verursachungsgerechten Angebotskalkulation von Blechteilen mit Hilfe wissensbasierter Methoden
LFT, 155 Seiten, 53 Bilder, 26 Tab. 1999.
ISBN 3-87525-130-X.

Band 99: Frank Breitenbach
Bildverarbeitungssystem zur Erfassung der Anschlußgeometrie elektronischer SMT-Bauelemente
LFT, 147 Seiten, 92 Bilder, 12 Tab. 2000.
ISBN 3-87525-131-8.

Band 100: Bernd Falk
Simulationsbasierte Lebensdauervorhersage für Werkzeuge der Kaltmassivumformung
LFT, 134 Seiten, 44 Bilder, 15 Tab. 2000.
ISBN 3-87525-136-9.

Band 101: Wolfgang Schlögl
Integriertes Simulationsdaten-Management für Maschinenentwicklung und Anlagenplanung
FAPS, 169 Seiten, 101 Bilder, 20 Tab. 2000.
ISBN 3-87525-137-7.

Band 102: Christian Hinsel
Ermüdungsbruchversagen hartstoffbeschichteter Werkzeugstähle in der Kaltmassivumformung
LFT, 130 Seiten, 80 Bilder, 14 Tab. 2000.
ISBN 3-87525-138-5.

Band 103: Stefan Bobbert
Simulationsgestützte Prozessauslegung für das Innenhochdruck-Umformen von Blechpaaren
LFT, 123 Seiten, 77 Bilder. 2000.
ISBN 3-87525-145-8.

Band 104: Harald Rottbauer
Modulares Planungswerkzeug zum Produktionsmanagement in der Elektronikproduktion
FAPS, 166 Seiten, 106 Bilder. 2001.
ISBN 3-87525-139-3.

Band 111: Jürgen Göhringer
Integrierte Telediagnose via Internet zum effizienten Service von Produktionssystemen
FAPS, 178 Seiten, 98 Bilder, 5 Tab. 2001.
ISBN 3-87525-147-4.

Band 105: Thomas Hennige
Flexible Formgebung von Blechen durch Laserstrahlumformen
LFT, 119 Seiten, 50 Bilder. 2001.
ISBN 3-87525-140-7.

Band 106: Thomas Menzel
Wissensbasierte Methoden für die rechnergestützte Charakterisierung und Bewertung innovativer Fertigungsprozesse
LFT, 152 Seiten, 71 Bilder. 2001.
ISBN 3-87525-142-3.

Band 107: Thomas Stöckel
Kommunikationstechnische Integration der Prozeßebene in Produktionssysteme durch Middleware-Frameworks
FAPS, 147 Seiten, 65 Bilder, 5 Tab. 2001.
ISBN 3-87525-143-1.

Band 108: Frank Pitter
Verfügbarkeitssteigerung von Werkzeugmaschinen durch Einsatz mechatronischer Sensorlösungen
FAPS, 158 Seiten, 131 Bilder, 8 Tab. 2001.
ISBN 3-87525-144-X.

Band 109: Markus Korneli
Integration lokaler CAP-Systeme in einen globalen Fertigungsdatenverbund
FAPS, 121 Seiten, 53 Bilder, 11 Tab. 2001.
ISBN 3-87525-146-6.

Band 110: Burkhard Müller
Laserstrahljustieren mit Excimer-Lasern - Prozeßparameter und Modelle zur Aktorkonstruktion
LFT, 128 Seiten, 36 Bilder, 9 Tab. 2001.
ISBN 3-87525-159-8.

Band 111: Jürgen Göhringer
Integrierte Telediagnose via Internet zum effizienten Service von Produktionssystemen
FAPS, 178 Seiten, 98 Bilder, 5 Tab. 2001.
ISBN 3-87525-147-4.

Band 112: Robert Feuerstein
Qualitäts- und kosteneffiziente Integration neuer Bauelementetechnologien in die Flachbaugruppenfertigung
FAPS, 161 Seiten, 99 Bilder, 10 Tab. 2001.
ISBN 3-87525-151-2.

Band 113: Marcus Reichenberger
Eigenschaften und Einsatzmöglichkeiten alternativer Elektroniklote in der Oberflächenmontage (SMT)
FAPS, 165 Seiten, 97 Bilder, 18 Tab. 2001.
ISBN 3-87525-152-0.

Band 114: Alexander Huber
Justieren vormontierter Systeme mit dem Nd:YAG-Laser unter Einsatz von Aktoren
LFT, 122 Seiten, 58 Bilder, 5 Tab. 2001.
ISBN 3-87525-153-9.

Band 115: Sami Krimi
Analyse und Optimierung von Montagesystemen in der Elektronikproduktion
FAPS, 155 Seiten, 88 Bilder, 3 Tab. 2001.
ISBN 3-87525-157-1.

Band 116: Marion Merklein
Laserstrahlumformen von Aluminiumwerkstoffen - Beeinflussung der Mikrostruktur und der mechanischen Eigenschaften
LFT, 122 Seiten, 65 Bilder, 15 Tab. 2001.
ISBN 3-87525-156-3.

Band 117: Thomas Collisi
Ein informationslogistisches Architekturkonzept zur Akquisition simulationsrelevanter Daten
FAPS, 181 Seiten, 105 Bilder, 7 Tab. 2002.
ISBN 3-87525-164-4.

Band 118: Markus Koch
Rationalisierung und ergonomische Optimierung im Innenausbau durch den Einsatz moderner Automatisierungstechnik
FAPS, 176 Seiten, 98 Bilder, 9 Tab. 2002.
ISBN 3-87525-165-2.

Band 119: Michael Schmidt
Prozeßregelung für das Laserstrahl-Punktschweißen in der Elektronikproduktion
LFT, 152 Seiten, 71 Bilder, 3 Tab. 2002.
ISBN 3-87525-166-0.

Band 120: Nicolas Tiesler
Grundlegende Untersuchungen zum Fließpressen metallischer Kleinstteile
LFT, 126 Seiten, 78 Bilder, 12 Tab. 2002.
ISBN 3-87525-175-X.

Band 121: Lars Pursche
Methoden zur technologieorientierten Programmierung für die 3D-Lasermikrobearbeitung
LFT, 111 Seiten, 39 Bilder, 0 Tab. 2002.
ISBN 3-87525-183-0.

Band 122: Jan-Oliver Brassel
Prozeßkontrolle beim Laserstrahl-Mikroschweißen
LFT, 148 Seiten, 72 Bilder, 12 Tab. 2002.
ISBN 3-87525-181-4.

Band 123: Mark Geisel
Prozeßkontrolle und -steuerung beim Laserstrahlschweißen mit den Methoden der nichtlinearen Dynamik
LFT, 135 Seiten, 46 Bilder, 2 Tab. 2002.
ISBN 3-87525-180-6.

Band 124: Gerd Eßer
Laserstrahlunterstützte Erzeugung metallischer Leiterstrukturen auf Thermoplastsubstraten für die MID-Technik
LFT, 148 Seiten, 60 Bilder, 6 Tab. 2002.
ISBN 3-87525-171-7.

Band 125: Marc Fleckenstein
Qualität laserstrahl-gefügter Mikroverbindungen elektronischer Kontakte
LFT, 159 Seiten, 77 Bilder, 7 Tab. 2002.
ISBN 3-87525-170-9.

Band 126: Stefan Kaufmann
Grundlegende Untersuchungen zum Nd:YAG- Laserstrahlfügen von Silizium für Komponenten der Optoelektronik
LFT, 159 Seiten, 100 Bilder, 6 Tab. 2002.
ISBN 3-87525-172-5.

Band 127: Thomas Fröhlich
Simultanes Löten von Anschlußkontakten elektronischer Bauelemente mit Diodenlaserstrahlung
LFT, 143 Seiten, 75 Bilder, 6 Tab. 2002.
ISBN 3-87525-186-5.

Band 128: Achim Hofmann
Erweiterung der Formgebungsgrenzen beim Umformen von Aluminiumwerkstoffen durch den Einsatz prozessangepasster Platinen
LFT, 113 Seiten, 58 Bilder, 4 Tab. 2002.
ISBN 3-87525-182-2.

Band 129: Ingo Kriebitzsch
3 - D MID Technologie in der Automobilelektronik
FAPS, 129 Seiten, 102 Bilder, 10 Tab. 2002.
ISBN 3-87525-169-5.

Band 130: Thomas Pohl
Fertigungsqualität und Umformbarkeit laserstrahlgeschweißter Formplatinen aus Aluminiumlegierungen
LFT, 133 Seiten, 93 Bilder, 12 Tab. 2002.
ISBN 3-87525-173-3.

Band 131: Matthias Wenk
Entwicklung eines konfigurierbaren Steuerungssystems für die flexible Sensorführung von Industrierobotern
FAPS, 167 Seiten, 85 Bilder, 1 Tab. 2002.
ISBN 3-87525-174-1.

Band 132: Matthias Negendanck
Neue Sensorik und Aktorik für Bearbeitungsköpfe zum Laserstrahlschweißen
LFT, 116 Seiten, 60 Bilder, 14 Tab. 2002.
ISBN 3-87525-184-9.

Band 133: Oliver Kreis
Integrierte Fertigung - Verfahrensintegration durch Innenhochdruck-Umformen, Trennen und Laserstrahlschweißen in einem Werkzeug sowie ihre tele- und multimediale Präsentation
LFT, 167 Seiten, 90 Bilder, 43 Tab. 2002.
ISBN 3-87525-176-8.

Band 134: Stefan Trautner
Technische Umsetzung produktbezogener Instrumente der Umweltpolitik bei Elektro- und Elektronikgeräten
FAPS, 179 Seiten, 92 Bilder, 11 Tab. 2002.
ISBN 3-87525-177-6.

Band 135: Roland Meier
Strategien für einen produktorientierten Einsatz räumlicher spritzgegossener Schaltungsträger (3-D MID)
FAPS, 155 Seiten, 88 Bilder, 14 Tab. 2002.
ISBN 3-87525-178-4.

Band 136: Jürgen Wunderlich
Kostensimulation - Simulationsbasierte Wirtschaftlichkeitsregelung komplexer Produktionssysteme
FAPS, 202 Seiten, 119 Bilder, 17 Tab. 2002.
ISBN 3-87525-179-2.

Band 137: Stefan Novotny
Innenhochdruck-Umformen von Blechen aus Aluminium- und Magnesiumlegierungen bei erhöhter Temperatur
LFT, 132 Seiten, 82 Bilder, 6 Tab. 2002.
ISBN 3-87525-185-7.

Band 138: Andreas Licha
Flexible Montageautomatisierung zur Komplettmontage flächenhafter Produktstrukturen durch kooperierende Industrieroboter
FAPS, 158 Seiten, 87 Bilder, 8 Tab. 2003.
ISBN 3-87525-189-X.

Band 139: Michael Eisenbarth
Beitrag zur Optimierung der Aufbau- und Verbindungstechnik für mechatronische Baugruppen
FAPS, 207 Seiten, 141 Bilder, 9 Tab. 2003.
ISBN 3-87525-190-3.

Band 140: Frank Christoph
Durchgängige simulationsgestützte Planung von Fertigungseinrichtungen der Elektronikproduktion
FAPS, 187 Seiten, 107 Bilder, 9 Tab. 2003.
ISBN 3-87525-191-1.

Band 141: Hinnerk Hagenah
Simulationsbasierte Bestimmung der zu erwartenden Maßhaltigkeit für das Blechbiegen
LFT, 131 Seiten, 36 Bilder, 26 Tab. 2003.
ISBN 3-87525-192-X.

Band 142: Ralf Eckstein
Scherschneiden und Biegen metallischer Kleinstteile - Materialeinfluss und Materialverhalten
LFT, 148 Seiten, 71 Bilder, 19 Tab. 2003.
ISBN 3-87525-193-8.

Band 143: Frank H. Meyer-Pittroff
Excimerlaserstrahlbiegen dünner metallischer Folien mit homogener Lichtlinie
LFT, 138 Seiten, 60 Bilder, 16 Tab. 2003.
ISBN 3-87525-196-2.

Band 144: Andreas Kach
Rechnergestützte Anpassung von Laserstrahlschneidbahnen an Bauteilabweichungen
LFT, 139 Seiten, 69 Bilder, 11 Tab. 2004.
ISBN 3-87525-197-0.

Band 145: Stefan Hierl
System- und Prozeßtechnik für das simultane Löten mit Diodenlaserstrahlung von elektronischen Bauelementen
LFT, 124 Seiten, 66 Bilder, 4 Tab. 2004.
ISBN 3-87525-198-9.

Band 146: Thomas Neudecker
Tribologische Eigenschaften keramischer Blechumformwerkzeuge- Einfluss einer Oberflächenendbearbeitung mittels Excimerlaserstrahlung
LFT, 166 Seiten, 75 Bilder, 26 Tab. 2004.
ISBN 3-87525-200-4.

Band 147: Ulrich Wenger
Prozessoptimierung in der Wickeltechnik durch innovative maschinenbauliche und regelungstechnische Ansätze
FAPS, 132 Seiten, 88 Bilder, 0 Tab. 2004.
ISBN 3-87525-203-9.

Band 148: Stefan Slama
Effizienzsteigerung in der Montage durch marktorientierte Montagestrukturen und erweiterte Mitarbeiterkompetenz
FAPS, 188 Seiten, 125 Bilder, 0 Tab. 2004.
ISBN 3-87525-204-7.

Band 149: Thomas Wurm
Laserstrahljustieren mittels Aktoren-Entwicklung von Konzepten und Methoden für die rechnerunterstützte Modellierung und Optimierung von komplexen Aktorsystemen in der Mikrotechnik
LFT, 122 Seiten, 51 Bilder, 9 Tab. 2004.
ISBN 3-87525-206-3.

Band 150: Martino Celeghini
Wirkmedienbasierte Blechumformung: Grundlagenuntersuchungen zum Einfluss von Werkstoff und Bauteilgeometrie
LFT, 146 Seiten, 77 Bilder, 6 Tab. 2004.
ISBN 3-87525-207-1.

Band 151: Ralph Hohenstein
Entwurf hochdynamischer Sensor- und Regelsysteme für die adaptive Laserbearbeitung
LFT, 282 Seiten, 63 Bilder, 16 Tab. 2004.
ISBN 3-87525-210-1.

Band 152: Angelika Hutterer
Entwicklung prozessüberwachender Regelkreise für flexible Formgebungsprozesse
LFT, 149 Seiten, 57 Bilder, 2 Tab. 2005.
ISBN 3-87525-212-8.

Band 153: Emil Egerer
Massivumformen metallischer Kleinstteile bei erhöhter Prozesstemperatur
LFT, 158 Seiten, 87 Bilder, 10 Tab. 2005.
ISBN 3-87525-213-6.

Band 154: Rüdiger Holzmann
Strategien zur nachhaltigen Optimierung von Qualität und Zuverlässigkeit in der Fertigung hochintegrierter Flachbaugruppen
FAPS, 186 Seiten, 99 Bilder, 19 Tab. 2005.
ISBN 3-87525-217-9.

Band 155: Marco Nock
Biegeumformen mit Elastomerwerkzeugen Modellierung, Prozessauslegung und Abgrenzung des Verfahrens am Beispiel des Rohrbiegens
LFT, 164 Seiten, 85 Bilder, 13 Tab. 2005.
ISBN 3-87525-218-7.

Band 156: Frank Niebling
Qualifizierung einer Prozesskette zum Laserstrahlsintern metallischer Bauteile
LFT, 148 Seiten, 89 Bilder, 3 Tab. 2005.
ISBN 3-87525-219-5.

Band 157: Markus Meiler
Großserientauglichkeit trockenschmierstoffbeschichteter Aluminiumbleche im Presswerk Grundlegende Untersuchungen zur Tribologie, zum Umformverhalten und Bauteilversuche
LFT, 104 Seiten, 57 Bilder, 21 Tab. 2005.
ISBN 3-87525-221-7.

Band 158: Agus Sutanto
Solution Approaches for Planning of Assembly Systems in Three-Dimensional Virtual Environments
FAPS, 169 Seiten, 98 Bilder, 3 Tab. 2005.
ISBN 3-87525-220-9.

Band 159: Matthias Boiger
Hochleistungssysteme für die Fertigung elektronischer Baugruppen auf der Basis flexibler Schaltungsträger
FAPS, 175 Seiten, 111 Bilder, 8 Tab. 2005.
ISBN 3-87525-222-5.

Band 160: Matthias Pitz
Laserunterstütztes Biegen höchstfester Mehrphasenstähle
LFT, 120 Seiten, 73 Bilder, 11 Tab. 2005.
ISBN 3-87525-223-3.

Band 161: Meik Vahl
Beitrag zur gezielten Beeinflussung des Werkstoffflusses beim Innenhochdruck-Umformen von Blechen
LFT, 165 Seiten, 94 Bilder, 15 Tab. 2005.
ISBN 3-87525-224-1.

Band 162: Peter K. Kraus
Plattformstrategien - Realisierung einer varianz- und kostenoptimierten Wertschöpfung
FAPS, 181 Seiten, 95 Bilder, 0 Tab. 2005.
ISBN 3-87525-226-8.

Band 163: Adrienn Cser
Laserstrahlschmelzabtrag - Prozessanalyse und -modellierung
LFT, 146 Seiten, 79 Bilder, 3 Tab. 2005.
ISBN 3-87525-227-6.

Band 164: Markus C. Hahn
Grundlegende Untersuchungen zur Herstellung von Leichtbauverbundstrukturen mit Aluminiumschaumkern
LFT, 143 Seiten, 60 Bilder, 16 Tab. 2005.
ISBN 3-87525-228-4.

Band 165: Gordana Michos
Mechatronische Ansätze zur Optimierung von Vorschubachsen
FAPS, 146 Seiten, 87 Bilder, 17 Tab. 2005.
ISBN 3-87525-230-6.

Band 166: Markus Stark
Auslegung und Fertigung hochpräziser Faser-Kollimator-Arrays
LFT, 158 Seiten, 115 Bilder, 11 Tab. 2005.
ISBN 3-87525-231-4.

Band 167: Yurong Zhou
Kollaboratives Engineering Management in der integrierten virtuellen Entwicklung der Anlagen für die Elektronikproduktion
FAPS, 156 Seiten, 84 Bilder, 6 Tab. 2005.
ISBN 3-87525-232-2.

Band 168: Werner Enser
Neue Formen permanenter und lösbarer elektrischer Kontaktierungen für mechatronische Baugruppen
FAPS, 190 Seiten, 112 Bilder, 5 Tab. 2005.
ISBN 3-87525-233-0.

Band 169: Katrin Melzer
Integrierte Produktpolitik bei elektrischen und elektronischen Geräten zur Optimierung des Product-Life-Cycle
FAPS, 155 Seiten, 91 Bilder, 17 Tab. 2005.
ISBN 3-87525-234-9.

Band 170: Alexander Putz
Grundlegende Untersuchungen zur Erfassung der realen Vorspannung von armierten Kaltfließpresswerkzeugen mittels Ultraschall
LFT, 137 Seiten, 71 Bilder, 15 Tab. 2006.
ISBN 3-87525-237-3.

Band 171: Martin Prechtl
Automatisiertes Schichtverfahren für metallische Folien - System- und Prozesstechnik
LFT, 154 Seiten, 45 Bilder, 7 Tab. 2006.
ISBN 3-87525-238-1.

Band 172: Markus Meidert
Beitrag zur deterministischen Lebensdauerabschätzung von Werkzeugen der Kaltmassivumformung
LFT, 131 Seiten, 78 Bilder, 9 Tab. 2006.
ISBN 3-87525-239-X.

Band 173: Bernd Müller
Robuste, automatisierte Montagesysteme durch adaptive Prozessführung und montageübergreifende Fehlerprävention am Beispiel flächiger Leichtbauteile
FAPS, 147 Seiten, 77 Bilder, 0 Tab. 2006.
ISBN 3-87525-240-3.

Band 174: Alexander Hofmann
Hybrides Laserdurchstrahlschweißen von Kunststoffen
LFT, 136 Seiten, 72 Bilder, 4 Tab. 2006.
ISBN 978-3-87525-243-9.

Band 175: Peter Wölflick
Innovative Substrate und Prozesse mit feinsten Strukturen für bleifreie Mechatronik-Anwendungen
FAPS, 177 Seiten, 148 Bilder, 24 Tab. 2006.
ISBN 978-3-87525-246-0.

Band 176: Attila Komlodi
Detection and Prevention of Hot Cracks during Laser Welding of Aluminium Alloys Using Advanced Simulation Methods
LFT, 155 Seiten, 89 Bilder, 14 Tab. 2006.
ISBN 978-3-87525-248-4.

Band 177: Uwe Popp
Grundlegende Untersuchungen zum Laserstrahlstrukturieren von Kaltmassivumformwerkzeugen
LFT, 140 Seiten, 67 Bilder, 16 Tab. 2006.
ISBN 978-3-87525-249-1.

Band 178: Veit Rückel
Rechnergestützte Ablaufplanung und Bahngenerierung Für kooperierende Industrieroboter
FAPS, 148 Seiten, 75 Bilder, 7 Tab. 2006.
ISBN 978-3-87525-250-7.

Band 179: Manfred Dirscherl
Nicht-thermische Mikrojustiertechnik mittels ultrakurzer Laserpulse
LFT, 154 Seiten, 69 Bilder, 10 Tab. 2007.
ISBN 978-3-87525-251-4.

Band 180: Yong Zhuo
Entwurf eines rechnergestützten integrierten Systems für Konstruktion und Fertigungsplanung räumlicher spritzgegossener Schaltungsträger (3D-MID)
FAPS, 181 Seiten, 95 Bilder, 5 Tab. 2007.
ISBN 978-3-87525-253-8.

Band 181: Stefan Lang
Durchgängige Mitarbeiterinformation zur Steigerung von Effizienz und Prozesssicherheit in der Produktion
FAPS, 172 Seiten, 93 Bilder. 2007.
ISBN 978-3-87525-257-6.

Band 182: Hans-Joachim Krauß
Laserstrahlinduzierte Pyrolyse präkeramischer Polymere
LFT, 171 Seiten, 100 Bilder. 2007.
ISBN 978-3-87525-258-3.

Band 183: Stefan Junker
Technologien und Systemlösungen für die flexibel automatisierte Bestückung permanent erregter Läufer mit oberflächenmontierten Dauermagneten
FAPS, 173 Seiten, 75 Bilder. 2007.
ISBN 978-3-87525-259-0.

Band 184: Rainer Kohlbauer
Wissensbasierte Methoden für die simulationsgestützte Auslegung wirkmedienbasierter Blechumformprozesse
LFT, 135 Seiten, 50 Bilder. 2007.
ISBN 978-3-87525-260-6.

Band 185: Klaus Lamprecht
Wirkmedienbasierte Umformung tiefgezogener Vorformen unter besonderer Berücksichtigung maßgeschneiderter Halbzeuge
LFT, 137 Seiten, 81 Bilder. 2007.
ISBN 978-3-87525-265-1.

Band 186: Bernd Zolleiß
Optimierte Prozesse und Systeme für die Bestückung mechatronischer Baugruppen
FAPS, 180 Seiten, 117 Bilder. 2007.
ISBN 978-3-87525-266-8.

Band 187: Michael Kerausch
Simulationsgestützte Prozessauslegung für das Umformen lokal wärmebehandelter Aluminiumplatinen
LFT, 146 Seiten, 76 Bilder, 7 Tab. 2007.
ISBN 978-3-87525-267-5.

Band 188: Matthias Weber
Unterstützung der Wandlungsfähigkeit von Produktionsanlagen durch innovative Softwaresysteme
FAPS, 183 Seiten, 122 Bilder, 3 Tab. 2007.
ISBN 978-3-87525-269-9.

Band 189: Thomas Frick
Untersuchung der prozessbestimmenden Strahl-Stoff-Wechselwirkungen beim Laserstrahlschweißen von Kunststoffen
LFT, 104 Seiten, 62 Bilder, 8 Tab. 2007.
ISBN 978-3-87525-268-2.

Band 190: Joachim Hecht
Werkstoffcharakterisierung und Prozessauslegung für die wirkmedienbasierte Doppelblech-Umformung von Magnesiumlegierungen
LFT, 107 Seiten, 91 Bilder, 2 Tab. 2007.
ISBN 978-3-87525-270-5.

Band 191: Ralf Völkl
Stochastische Simulation zur Werkzeuglebensdaueroptimierung und Präzisionsfertigung in der Kaltmassivumformung
LFT, 178 Seiten, 75 Bilder, 12 Tab. 2008.
ISBN 978-3-87525-272-9.

Band 192: Massimo Tolazzi
Innenhochdruck-Umformen verstärkter Blech-Rahmenstrukturen
LFT, 164 Seiten, 85 Bilder, 7 Tab. 2008.
ISBN 978-3-87525-273-6.

Band 193: Cornelia Hoff
Untersuchung der Prozesseinflussgrößen beim Presshärten des höchstfesten Vergütungsstahls 22MnB5
LFT, 133 Seiten, 92 Bilder, 5 Tab. 2008.
ISBN 978-3-87525-275-0.

Band 194: Christian Alvarez
Simulationsgestützte Methoden zur effizienten Gestaltung von Lötprozessen in der Elektronikproduktion
FAPS, 149 Seiten, 86 Bilder, 8 Tab. 2008.
ISBN 978-3-87525-277-4.

Band 195: Andreas Kunze
Automatisierte Montage von makromechatronischen Modulen zur flexiblen Integration in hybride Pkw-Bordnetzsysteme
FAPS, 160 Seiten, 90 Bilder, 14 Tab. 2008.
ISBN 978-3-87525-278-1.

Band 196: Wolfgang Hußnätter
Grundlegende Untersuchungen zur experimentellen Ermittlung und zur Modellierung von Fließortkurven bei erhöhten Temperaturen
LFT, 152 Seiten, 73 Bilder, 21 Tab. 2008.
ISBN 978-3-87525-279-8.

Band 197: Thomas Bigl
Entwicklung, angepasste Herstellungsverfahren und erweiterte Qualitätssicherung von einsatzgerechten elektronischen Baugruppen
FAPS, 175 Seiten, 107 Bilder, 14 Tab. 2008.
ISBN 978-3-87525-280-4.

Band 198: Stephan Roth
Grundlegende Untersuchungen zum Excimerlaserstrahl-Abtragen unter Flüssigkeitsfilmen
LFT, 113 Seiten, 47 Bilder, 14 Tab. 2008.
ISBN 978-3-87525-281-1.

Band 199: Artur Giera
Prozesstechnische Untersuchungen zum Rührreibschweißen metallischer Werkstoffe
LFT, 179 Seiten, 104 Bilder, 36 Tab. 2008.
ISBN 978-3-87525-282-8.

Band 200: Jürgen Lechler
Beschreibung und Modellierung des Werkstoffverhaltens von presshärtbaren Bor-Manganstählen
LFT, 154 Seiten, 75 Bilder, 12 Tab. 2009.
ISBN 978-3-87525-286-6.

Band 201: Andreas Blankl
Untersuchungen zur Erhöhung der Prozessrobustheit bei der Innenhochdruck-Umformung von flächigen Halbzeugen mit vor- bzw. nachgeschalteten Laserstrahlfügeoperationen
LFT, 120 Seiten, 68 Bilder, 9 Tab. 2009.
ISBN 978-3-87525-287-3.

Band 202: Andreas Schaller
Modellierung eines nachfrageorientierten Produktionskonzeptes für mobile Telekommunikationsgeräte
FAPS, 120 Seiten, 79 Bilder, 0 Tab. 2009.
ISBN 978-3-87525-289-7.

Band 203: Claudius Schimpf
Optimierung von Zuverlässigkeitsuntersuchungen, Prüfabläufen und Nacharbeitsprozessen in der Elektronikproduktion
FAPS, 162 Seiten, 90 Bilder, 14 Tab. 2009.
ISBN 978-3-87525-290-3.

Band 204: Simon Dietrich
Sensoriken zur Schwerpunktslagebestimmung der optischen Prozessemissionen beim Laserstrahltiefschweißen
LFT, 138 Seiten, 70 Bilder, 5 Tab. 2009.
ISBN 978-3-87525-292-7.

Band 205: Wolfgang Wolf
Entwicklung eines agentenbasierten Steuerungssystems zur Materialflussorganisation im wandelbaren Produktionsumfeld
FAPS, 167 Seiten, 98 Bilder. 2009.
ISBN 978-3-87525-293-4.

Band 206: Steffen Polster
Laserdurchstrahlschweißen transparenter Polymerbauteile
LFT, 160 Seiten, 92 Bilder, 13 Tab. 2009.
ISBN 978-3-87525-294-1.

Band 207: Stephan Manuel Dörfler
Rührreibschweißen von walzplattiertem Halbzeug und Aluminiumblech zur Herstellung flächiger Aluminiumschaum-Sandwich-Verbundstrukturen
LFT, 190 Seiten, 98 Bilder, 5 Tab. 2009.
ISBN 978-3-87525-295-8.

Band 208: Uwe Vogt
Seriennahe Auslegung von Aluminium Tailored Heat Treated Blanks
LFT, 151 Seiten, 68 Bilder, 26 Tab. 2009.
ISBN 978-3-87525-296-5.

Band 209: Till Laumann
Qualitative und quantitative Bewertung der Crashtauglichkeit von höchstfesten Stählen
LFT, 117 Seiten, 69 Bilder, 7 Tab. 2009.
ISBN 978-3-87525-299-6.

Band 210: Alexander Diehl
Größeneffekte bei Biegeprozessen- Entwicklung einer Methodik zur Identifikation und Quantifizierung
LFT, 180 Seiten, 92 Bilder, 12 Tab. 2010.
ISBN 978-3-87525-302-3.

Band 211: Detlev Staud
Effiziente Prozesskettenauslegung für das Umformen lokal wärmebehandelter und geschweißter Aluminiumbleche
LFT, 164 Seiten, 72 Bilder, 12 Tab. 2010.
ISBN 978-3-87525-303-0.

Band 212: Jens Ackermann
Prozesssicherung beim Laserdurchstrahlschweißen thermoplastischer Kunststoffe
LPT, 129 Seiten, 74 Bilder, 13 Tab. 2010.
ISBN 978-3-87525-305-4.

Band 213: Stephan Weidel
Grundlegende Untersuchungen zum Kontaktzustand zwischen Werkstück und Werkzeug bei umformtechnischen Prozessen unter tribologischen Gesichtspunkten
LFT, 144 Seiten, 67 Bilder, 11 Tab. 2010.
ISBN 978-3-87525-307-8.

Band 214: Stefan Geißdörfer
Entwicklung eines mesoskopischen Modells zur Abbildung von Größeneffekten in der Kaltmassivumformung mit Methoden der FE-Simulation
LFT, 133 Seiten, 83 Bilder, 11 Tab. 2010.
ISBN 978-3-87525-308-5.

Band 215: Christian Matzner
Konzeption produktspezifischer Lösungen zur Robustheitssteigerung elektronischer Systeme gegen die Einwirkung von Betauung im Automobil
FAPS, 165 Seiten, 93 Bilder, 14 Tab. 2010.
ISBN 978-3-87525-309-2.

Band 216: Florian Schüßler
Verbindungs- und Systemtechnik für thermisch hochbeanspruchte und miniaturisierte elektronische Baugruppen
FAPS, 184 Seiten, 93 Bilder, 18 Tab. 2010.
ISBN 978-3-87525-310-8.

Band 217: Massimo Cojutti
Strategien zur Erweiterung der Prozessgrenzen bei der Innhochdruck-Umformung von Rohren und Blechpaaren
LFT, 125 Seiten, 56 Bilder, 9 Tab. 2010.
ISBN 978-3-87525-312-2.

Band 218: Raoul Plettke
Mehrkriterielle Optimierung komplexer Aktorsysteme für das Laserstrahljustieren
LFT, 152 Seiten, 25 Bilder, 3 Tab. 2010.
ISBN 978-3-87525-315-3.

Band 219: Andreas Dobroschke
Flexible Automatisierungslösungen für die Fertigung wickeltechnischer Produkte
FAPS, 184 Seiten, 109 Bilder, 18 Tab. 2011.
ISBN 978-3-87525-317-7.

Band 220: Azhar Zam
Optical Tissue Differentiation for Sensor-Controlled Tissue-Specific Laser Surgery
LPT, 99 Seiten, 45 Bilder, 8 Tab. 2011.
ISBN 978-3-87525-318-4.

Band 221: Michael Rösch
Potenziale und Strategien zur Optimierung des Schablonendruckprozesses in der Elektronikproduktion
FAPS, 192 Seiten, 127 Bilder, 19 Tab. 2011.
ISBN 978-3-87525-319-1.

Band 222: Thomas Rechtenwald
Quasi-isothermes Laserstrahlsintern von Hochtemperatur-Thermoplasten - Eine Betrachtung werkstoff-prozessspezifischer Aspekte am Beispiel PEEK
LPT, 150 Seiten, 62 Bilder, 8 Tab. 2011.
ISBN 978-3-87525-320-7.

Band 223: Daniel Craiovan
Prozesse und Systemlösungen für die SMT-Montage optischer Bauelemente auf Substrate mit integrierten Lichtwellenleitern
FAPS, 165 Seiten, 85 Bilder, 8 Tab. 2011.
ISBN 978-3-87525-324-5.

Band 224: Kay Wagner
Beanspruchungsangepasste Kaltmassivumformwerkzeuge durch lokal optimierte Werkzeugoberflächen
LFT, 147 Seiten, 103 Bilder, 17 Tab. 2011.
ISBN 978-3-87525-325-2.

Band 225: Martin Brandhuber
Verbesserung der Prognosegüte des Versagens von Punktschweißverbindungen bei höchstfesten Stahlgüten
LFT, 155 Seiten, 91 Bilder, 19 Tab. 2011.
ISBN 978-3-87525-327-6.

Band 226: Peter Sebastian Feuser
Ein Ansatz zur Herstellung von pressgehärteten Karosseriekomponenten mit maßgeschneiderten mechanischen Eigenschaften: Temperierte Umformwerkzeuge. Prozessfenster, Prozesssimulation und funktionale Untersuchung
LFT, 195 Seiten, 97 Bilder, 60 Tab. 2012.
ISBN 978-3-87525-328-3.

Band 227: Murat Arbak
Material Adapted Design of Cold Forging Tools Exemplified by Powder Metallurgical Tool Steels and Ceramics
LFT, 109 Seiten, 56 Bilder, 8 Tab. 2012.
ISBN 978-3-87525-330-6.

Band 228: Indra Pitz
Beschleunigte Simulation des Laserstrahlumformens von Aluminiumblechen
LPT, 137 Seiten, 45 Bilder, 27 Tab. 2012.
ISBN 978-3-87525-333-7.

Band 229: Alexander Grimm
Prozessanalyse und -überwachung des Laserstrahlhartlötens mittels optischer Sensorik
LPT, 125 Seiten, 61 Bilder, 5 Tab. 2012.
ISBN 978-3-87525-334-4.

Band 230: Markus Kaupper
Biegen von höhenfesten Stahlblechwerkstoffen - Umformverhalten und Grenzen der Biegbarkeit
LFT, 160 Seiten, 57 Bilder, 10 Tab. 2012.
ISBN 978-3-87525-339-9.

Band 231: Thomas Kroiß
Modellbasierte Prozessauslegung für die Kaltmassivumformung unter Brücksichtigung der Werkzeug- und Pressenauffederung
LFT, 169 Seiten, 50 Bilder, 19 Tab. 2012.
ISBN 978-3-87525-341-2.

Band 232: Christian Goth
Analyse und Optimierung der Entwicklung und Zuverlässigkeit räumlicher Schaltungsträger (3D-MID)
FAPS, 176 Seiten, 102 Bilder, 22 Tab. 2012.
ISBN 978-3-87525-340-5.

Band 233: Christian Ziegler
Ganzheitliche Automatisierung mechatronischer Systeme in der Medizin am Beispiel Strahlentherapie
FAPS, 170 Seiten, 71 Bilder, 19 Tab. 2012.
ISBN 978-3-87525-342-9.

Band 234: Florian Albert
Automatisiertes Laserstrahllöten und -reparaturlöten elektronischer Baugruppen
LPT, 127 Seiten, 78 Bilder, 11 Tab. 2012.
ISBN 978-3-87525-344-3.

Band 235: Thomas Stöhr
Analyse und Beschreibung des mechanischen Werkstoffverhaltens von presshärtbaren Bor-Manganstählen
LFT, 118 Seiten, 74 Bilder, 18 Tab. 2013.
ISBN 978-3-87525-346-7.

Band 236: Christian Kägeler
Prozessdynamik beim Laserstrahlschweißen verzinkter Stahlbleche im Überlappstoß
LPT, 145 Seiten, 80 Bilder, 3 Tab. 2013.
ISBN 978-3-87525-347-4.

Band 237: Andreas Sulzberger
Seriennahe Auslegung der Prozesskette zur wärmeunterstützten Umformung von Aluminiumblechwerkstoffen
LFT, 153 Seiten, 87 Bilder, 17 Tab. 2013.
ISBN 978-3-87525-349-8.

Band 238: Simon Opel
Herstellung prozessangepasster Halbzeuge mit variabler Blechdicke durch die Anwendung von Verfahren der Blechmassivumformung
LFT, 165 Seiten, 108 Bilder, 27 Tab. 2013.
ISBN 978-3-87525-350-4.

Band 239: Rajesh Kanawade
In-vivo Monitoring of Epithelium Vessel and Capillary Density for the Application of Detection of Clinical Shock and Early Signs of Cancer Development
LPT, 124 Seiten, 58 Bilder, 15 Tab. 2013.
ISBN 978-3-87525-351-1.

Band 240: Stephan Busse
Entwicklung und Qualifizierung eines Schneidclinchverfahrens
LFT, 119 Seiten, 86 Bilder, 20 Tab. 2013.
ISBN 978-3-87525-352-8.

Band 241: Karl-Heinz Leitz
Mikro- und Nanostrukturierung mit kurz und ultrakurz gepulster Laserstrahlung
LPT, 154 Seiten, 71 Bilder, 9 Tab. 2013.
ISBN 978-3-87525-355-9.

Band 242: Markus Michl
Webbasierte Ansätze zur ganzheitlichen technischen Diagnose
FAPS, 182 Seiten, 62 Bilder, 20 Tab. 2013.
ISBN 978-3-87525-356-6.

Band 243: Vera Sturm
Einfluss von Chargenschwankungen auf die Verarbeitungsgrenzen von Stahlwerkstoffen
LFT, 113 Seiten, 58 Bilder, 9 Tab. 2013.
ISBN 978-3-87525-357-3.

Band 244: Christian Neudel
Mikrostrukturelle und mechanisch-technologische Eigenschaften widerstandspunktgeschweißter Aluminium-Stahl-Verbindungen für den Fahrzeugbau
LFT, 178 Seiten, 171 Bilder, 31 Tab. 2014.
ISBN 978-3-87525-358-0.

Band 245: Anja Neumann
Konzept zur Beherrschung der Prozessschwankungen im Presswerk
LFT, 162 Seiten, 68 Bilder, 15 Tab. 2014.
ISBN 978-3-87525-360-3.

Band 246: Ulf-Hermann Quentin
Laserbasierte Nanostrukturierung mit optisch positionierten Mikrolinsen
LPT, 137 Seiten, 89 Bilder, 6 Tab. 2014.
ISBN 978-3-87525-361-0.

Band 247: Erik Lamprecht
Der Einfluss der Fertigungsverfahren auf die Wirbelstromverluste von Stator-Einzelzahnblechpaketen für den Einsatz in Hybrid- und Elektrofahrzeugen
FAPS, 148 Seiten, 138 Bilder, 4 Tab. 2014.
ISBN 978-3-87525-362-7.

Band 248: Sebastian Rösel
Wirkmedienbasierte Umformung von Blechhalbzeugen unter Anwendung magnetorheologischer Flüssigkeiten als kombiniertes Wirk- und Dichtmedium
LFT, 148 Seiten, 61 Bilder, 12 Tab. 2014.
ISBN 978-3-87525-363-4.

Band 249: Paul Hippchen
Simulative Prognose der Geometrie indirekt pressgehärteter Karosseriebauteile für die industrielle Anwendung
LFT, 163 Seiten, 89 Bilder, 12 Tab. 2014.
ISBN 978-3-87525-364-1.

Band 250: Martin Zubeil
Versagensprognose bei der Prozesssimulation von Biegeumform- und Falzverfahren
LFT, 171 Seiten, 90 Bilder, 5 Tab. 2014.
ISBN 978-3-87525-365-8.

Band 251: Alexander Kühl
Flexible Automatisierung der Statorenmontage mit Hilfe einer universellen ambidexteren Kinematik
FAPS, 142 Seiten, 60 Bilder, 26 Tab. 2014.
ISBN 978-3-87525-367-2.

Band 252: Thomas Albrecht
Optimierte Fertigungstechnologien für Rotoren getriebeintegrierter PM-Synchronmotoren von Hybridfahrzeugen
FAPS, 198 Seiten, 130 Bilder, 38 Tab. 2014.
ISBN 978-3-87525-368-9.

Band 253: Florian Risch
Planning and Production Concepts for Contactless Power Transfer Systems for Electric Vehicles
FAPS, 185 Seiten, 125 Bilder, 13 Tab. 2014.
ISBN 978-3-87525-369-6.

Band 254: Markus Weigl
Laserstrahlschweißen von Mischverbindungen aus austenitischen und ferritischen korrosionsbeständigen Stahlwerkstoffen
LPT, 184 Seiten, 110 Bilder, 6 Tab. 2014.
ISBN 978-3-87525-370-2.

Band 255: Johannes Noneder
Beanspruchungserfassung für die Validierung von FE-Modellen zur Auslegung von Massivumformwerkzeugen
LFT, 161 Seiten, 65 Bilder, 14 Tab. 2014.
ISBN 978-3-87525-371-9.

Band 256: Andreas Reinhardt
Ressourceneffiziente Prozess- und Produktionstechnologie für flexible Schaltungsträger
FAPS, 123 Seiten, 69 Bilder, 19 Tab. 2014.
ISBN 978-3-87525-373-3.

Band 257: Tobias Schmuck
Ein Beitrag zur effizienten Gestaltung globaler Produktions- und Logistiknetzwerke mittels Simulation
FAPS, 151 Seiten, 74 Bilder. 2014.
ISBN 978-3-87525-374-0.

Band 258: Bernd Eichenhüller
Untersuchungen der Effekte und Wechselwirkungen charakteristischer Einflussgrößen auf das Umformverhalten bei Mikroumformprozessen
LFT, 127 Seiten, 29 Bilder, 9 Tab. 2014.
ISBN 978-3-87525-375-7.

Band 259: Felix Lütteke
Vielseitiges autonomes Transportsystem basierend auf Weltmodellerstellung mittels Datenfusion von Deckenkameras und Fahrzeugsensoren
FAPS, 152 Seiten, 54 Bilder, 20 Tab. 2014.
ISBN 978-3-87525-376-4.

Band 260: Martin Grüner
Hochdruck-Blechumformung mit formlos festen Stoffen als Wirkmedium
LFT, 144 Seiten, 66 Bilder, 29 Tab. 2014.
ISBN 978-3-87525-379-5.

Band 261: Christian Brock
Analyse und Regelung des Laserstrahltiefschweißprozesses durch Detektion der Metalldampffackelposition
LPT, 126 Seiten, 65 Bilder, 3 Tab. 2015.
ISBN 978-3-87525-380-1.

Band 262: Peter Vatter
Sensitivitätsanalyse des 3-Rollen-Schubbiegens auf Basis der Finite Elemente Methode
LFT, 145 Seiten, 57 Bilder, 26 Tab. 2015.
ISBN 978-3-87525-381-8.

Band 263: Florian Klämpfl
Planung von Laserbestrahlungen durch simulationsbasierte Optimierung
LPT, 169 Seiten, 78 Bilder, 32 Tab. 2015.
ISBN 978-3-87525-384-9.

Band 264: Matthias Domke
Transiente physikalische Mechanismen bei der Laserablation von dünnen Metallschichten
LPT, 133 Seiten, 43 Bilder, 3 Tab. 2015.
ISBN 978-3-87525-385-6.

Band 265: Johannes Götz
Community-basierte Optimierung des Anlagenengineerings
FAPS, 177 Seiten, 80 Bilder, 30 Tab. 2015.
ISBN 978-3-87525-386-3.

Band 266: Hung Nguyen
Qualifizierung des Potentials von Verfestigungseffekten zur Erweiterung des Umformvermögens aushärtbarer Aluminiumlegierungen
LFT, 137 Seiten, 57 Bilder, 16 Tab. 2015.
ISBN 978-3-87525-387-0.

Band 267: Andreas Kuppert
Erweiterung und Verbesserung von Versuchs- und Auswertetechniken für die Bestimmung von Grenzformänderungskurven
LFT, 138 Seiten, 82 Bilder, 2 Tab. 2015.
ISBN 978-3-87525-388-7.

Band 268: Kathleen Klaus
Erstellung eines Werkstofforientierten Fertigungsprozessfensters zur Steigerung des Formgebungsvermögens von Aluminiumlegierungen unter Anwendung einer zwischengeschalteten Wärmebehandlung
LFT, 154 Seiten, 70 Bilder, 8 Tab. 2015.
ISBN 978-3-87525-391-7.

Band 269: Thomas Svec
Untersuchungen zur Herstellung von funktionsoptimierten Bauteilen im partiellen Presshärtprozess mittels lokal unterschiedlich temperierter Werkzeuge
LFT, 166 Seiten, 87 Bilder, 15 Tab. 2015.
ISBN 978-3-87525-392-4.

Band 270: Tobias Schrader
Grundlegende Untersuchungen zur Verschleißcharakterisierung beschichteter Kaltmassivumformwerkzeuge
LFT, 164 Seiten, 55 Bilder, 11 Tab. 2015.
ISBN 978-3-87525-393-1.

Band 271: Matthäus Brela
Untersuchung von Magnetfeld-Messmethoden zur ganzheitlichen Wertschöpfungsoptimierung und Fehlerdetektion an magnetischen Aktoren
FAPS, 170 Seiten, 97 Bilder, 4 Tab. 2015.
ISBN 978-3-87525-394-8.

Band 272: Michael Wieland
Entwicklung einer Methode zur Prognose adhäsiven Verschleißes an Werkzeugen für das direkte Presshärten
LFT, 156 Seiten, 84 Bilder, 9 Tab. 2015.
ISBN 978-3-87525-395-5.

Band 273: René Schramm
Strukturierte additive Metallisierung durch kaltaktives Atmosphärendruckplasma
FAPS, 136 Seiten, 62 Bilder, 15 Tab. 2015.
ISBN 978-3-87525-396-2.

Band 274: Michael Lechner
Herstellung beanspruchungsangepasster Aluminiumblechhalbzeuge durch eine maßgeschneiderte Variation der Abkühlgeschwindigkeit nach Lösungsglühen
LFT, 136 Seiten, 62 Bilder, 15 Tab. 2015.
ISBN 978-3-87525-397-9.

Band 275: Kolja Andreas
Einfluss der Oberflächenbeschaffenheit auf das Werkzeugeinsatzverhalten beim Kaltfließpressen
LFT, 169 Seiten, 76 Bilder, 4 Tab. 2015.
ISBN 978-3-87525-398-6.

Band 276: Marcus Baum
Laser Consolidation of ITO Nanoparticles for the Generation of Thin Conductive Layers on Transparent Substrates
LPT, 158 Seiten, 75 Bilder, 3 Tab. 2015.
ISBN 978-3-87525-399-3.

Band 277: Thomas Schneider
Umformtechnische Herstellung dünnwandiger Funktionsbauteile aus Feinblech durch Verfahren der Blechmassivumformung
LFT, 188 Seiten, 95 Bilder, 7 Tab. 2015.
ISBN 978-3-87525-401-3.

Band 278: Jochen Merhof
Sematische Modellierung automatisierter Produktionssysteme zur Verbesserung der IT-Integration zwischen Anlagen-Engineering und Steuerungsebene
FAPS, 157 Seiten, 88 Bilder, 8 Tab. 2015.
ISBN 978-3-87525-402-0.

Band 279: Fabian Zöller
Erarbeitung von Grundlagen zur Abbildung des tribologischen Systems in der Umformsimulation
LFT, 126 Seiten, 51 Bilder, 3 Tab. 2016.
ISBN 978-3-87525-403-7.

Band 280: Christian Hezler
Einsatz technologischer Versuche zur Erweiterung der Versagensvorhersage bei Karosseriebauteilen aus höchstfesten Stählen
LFT, 147 Seiten, 63 Bilder, 44 Tab. 2016.
ISBN 978-3-87525-404-4.

Band 281: Jochen Bönig
Integration des Systemverhaltens von Automobil-Hochvoltleitungen in die virtuelle Absicherung durch strukturmechanische Simulation
FAPS, 177 Seiten, 107 Bilder, 17 Tab. 2016.
ISBN 978-3-87525-405-1.

Band 282: Johannes Kohl
Automatisierte Datenerfassung für diskret ereignisorientierte Simulationen in der energieflexibelen Fabrik
FAPS, 160 Seiten, 80 Bilder, 27 Tab. 2016.
ISBN 978-3-87525-406-8.

Band 283: Peter Bechtold
Mikroschockwellenumformung mittels ultrakurzer Laserpulse
LPT, 155 Seiten, 59 Bilder, 10 Tab. 2016.
ISBN 978-3-87525-407-5.

Band 284: Stefan Berger
Laserstrahlschweißen thermoplastischer Kohlenstofffaserverbundwerkstoffe mit spezifischem Zusatzdraht
LPT, 118 Seiten, 68 Bilder, 9 Tab. 2016.
ISBN 978-3-87525-408-2.

Band 285: Martin Bornschlegl
Methods-Energy Measurement - Eine Methode zur Energieplanung für Fügeverfahren im Karosseriebau
FAPS, 136 Seiten, 72 Bilder, 46 Tab. 2016.
ISBN 978-3-87525-409-9.

Band 286: Tobias Rackow
Erweiterung des Unternehmenscontrollings um die Dimension Energie
FAPS, 164 Seiten, 82 Bilder, 29 Tab. 2016.
ISBN 978-3-87525-410-5.

Band 287: Johannes Koch
Grundlegende Untersuchungen zur Herstellung zyklisch-symmetrischer Bauteile mit Nebenformelementen durch Blechmassivumformung
LFT, 125 Seiten, 49 Bilder, 17 Tab. 2016.
ISBN 978-3-87525-411-2.

Band 288: Hans Ulrich Vierzigmann
Beitrag zur Untersuchung der tribologischen Bedingungen in der Blechmassivumformung - Bereitstellung von tribologischen Modellversuchen und Realisierung von Tailored Surfaces
LFT, 174 Seiten, 102 Bilder, 34 Tab. 2016.
ISBN 978-3-87525-412-9.

Band 289: Thomas Senner
Methodik zur virtuellen Absicherung der formgebenden Operation des Nasspressprozesses von Gelege-Mehrschichtverbunden
LFT, 156 Seiten, 96 Bilder, 21 Tab. 2016.
ISBN 978-3-87525-414-3.

Band 290: Sven Kreitlein
Der grundoperationsspezifische Mindestenergiebedarf als Referenzwert zur Bewertung der Energieeffizienz in der Produktion
FAPS, 185 Seiten, 64 Bilder, 30 Tab. 2016.
ISBN 978-3-87525-415-0.

Band 291: Christian Roos
Remote-Laserstrahlschweißen verzinkter Stahlbleche in Kehlnahtgeometrie
LPT, 123 Seiten, 52 Bilder, 0 Tab. 2016.
ISBN 978-3-87525-416-7.

Band 292: Alexander Kahrimanidis
Thermisch unterstützte Umformung von Aluminiumblechen
LFT, 165 Seiten, 103 Bilder, 18 Tab. 2016.
ISBN 978-3-87525-417-4.

Band 293: Jan Tremel
Flexible Systems for Permanent Magnet Assembly and Magnetic Rotor Measurement / Flexible Systeme zur Montage von Permanentmagneten und zur Messung magnetischer Rotoren
FAPS, 152 Seiten, 91 Bilder, 12 Tab. 2016.
ISBN 978-3-87525-419-8.

Band 294: Ioannis Tsoupis
Schädigungs- und Versagensverhalten hochfester Leichtbauwerkstoffe unter Biegebeanspruchung
LFT, 176 Seiten, 51 Bilder, 6 Tab. 2017.
ISBN 978-3-87525-420-4.

Band 295: Sven Hildering
Grundlegende Untersuchungen zum Prozessverhalten von Silizium als Werkzeugwerkstoff für das Mikroscherschneiden metallischer Folien
LFT, 177 Seiten, 74 Bilder, 17 Tab. 2017.
ISBN 978-3-87525-422-8.

Band 296: Sasia Mareike Hertweck
Zeitliche Pulsformung in der Lasermikromaterialbearbeitung – Grundlegende Untersuchungen und Anwendungen
LPT, 146 Seiten, 67 Bilder, 5 Tab. 2017.
ISBN 978-3-87525-423-5.

Band 297: Paryanto
Mechatronic Simulation Approach for the Process Planning of Energy-Efficient Handling Systems
FAPS, 162 Seiten, 86 Bilder, 13 Tab. 2017.
ISBN 978-3-87525-424-2.

Band 298: Peer Stenzel
Großserientaugliche Nadelwickeltechnik für verteilte Wicklungen im Anwendungsfall der E-Traktionsantriebe
FAPS, 239 Seiten, 147 Bilder, 20 Tab. 2017.
ISBN 978-3-87525-425-9.

Band 299: Mario Lušić
Ein Vorgehensmodell zur Erstellung montageführender Werkerinformationssysteme simultan zum Produktentstehungsprozess
FAPS, 174 Seiten, 79 Bilder, 22 Tab. 2017.
ISBN 978-3-87525-426-6.

Band 300: Arnd Buschhaus
Hochpräzise adaptive Steuerung und Regelung robotergeführter Prozesse
FAPS, 202 Seiten, 96 Bilder, 4 Tab. 2017.
ISBN 978-3-87525-427-3.

Band 301: Tobias Laumer
Erzeugung von thermoplastischen Werkstoffverbunden mittels simultanem, intensitätsselektivem Laserstrahlschmelzen
LPT, 140 Seiten, 82 Bilder, 0 Tab. 2017.
ISBN 978-3-87525-428-0.

Band 302: Nora Unger
Untersuchung einer thermisch unterstützten Fertigungskette zur Herstellung umgeformter Bauteile aus der höherfesten Aluminiumlegierung EN AW-7020
LFT, 142 Seiten, 53 Bilder, 8 Tab. 2017.
ISBN 978-3-87525-429-7.

Band 303: Tommaso Stellin
Design of Manufacturing Processes for the Cold Bulk Forming of Small Metal Components from Metal Strip
LFT, 146 Seiten, 67 Bilder, 7 Tab. 2017.
ISBN 978-3-87525-430-3.

Band 304: Bassim Bachy
Experimental Investigation, Modeling, Simulation and Optimization of Molded Interconnect Devices (MID) Based on Laser Direct Structuring (LDS) / Experimentelle Untersuchung, Modellierung, Simulation und Optimierung von Molded Interconnect Devices (MID) basierend auf Laser Direktstrukturierung (LDS)
FAPS, 168 Seiten, 120 Bilder, 26 Tab. 2017.
ISBN 978-3-87525-431-0.

Band 305: Michael Spahr
Automatisierte Kontaktierungsverfahren für flachleiterbasierte Pkw-Bordnetzsysteme
FAPS, 197 Seiten, 98 Bilder, 17 Tab. 2017.
ISBN 978-3-87525-432-7.

Band 306: Sebastian Suttner
Charakterisierung und Modellierung des spannungszustandsabhängigen Werkstoffverhaltens der Magnesiumlegierung AZ31B für die numerische Prozessauslegung
LFT, 150 Seiten, 84 Bilder, 19 Tab. 2017.
ISBN 978-3-87525-433-4.

Band 307: Bhargav Potdar
A reliable methodology to deduce thermo-mechanical flow behaviour of hot stamping steels
LFT, 203 Seiten, 98 Bilder, 27 Tab. 2017.
ISBN 978-3-87525-436-5.

Band 308: Maria Löffler
Steuerung von Blechmassivumformprozessen durch maßgeschneiderte tribologische Systeme
LFT, viii u. 166 Seiten, 90 Bilder, 5 Tab. 2018. ISBN 978-3-96147-133-1.

Band 309: Martin Müller
Untersuchung des kombinierten Trenn- und Umformprozesses beim Fügen artungleicher Werkstoffe mittels Schneidclinchverfahren
LFT, xi u. 149 Seiten, 89 Bilder, 6 Tab. 2018. ISBN: 978-3-96147-135-5.

Band 310: Christopher Kästle
Qualifizierung der Kupfer-Drahtbondtechnologie für integrierte Leistungsmodule in harschen Umgebungsbedingungen
FAPS, xii u. 167 Seiten, 70 Bilder, 18 Tab. 2018. ISBN 978-3-96147-145-4.

Band 311: Daniel Vipavc
Eine Simulationsmethode für das 3-Rollen-Schubbiegen
LFT, xiii u. 121 Seiten, 56 Bilder, 17 Tab. 2018. ISBN 978-3-96147-147-8.

Band 312: Christina Ramer
Arbeitsraumüberwachung und autonome Bahnplanung für ein sicheres und flexibles Roboter-Assistenzsystem in der Fertigung
FAPS, xiv u. 188 Seiten, 57 Bilder, 9 Tab. 2018. ISBN 978-3-96147-153-9.

Band 313: Miriam Rauer
Der Einfluss von Poren auf die Zuverlässigkeit der Lötverbindungen von Hochleistungs-Leuchtdioden
FAPS, xii u. 209 Seiten, 108 Bilder, 21 Tab. 2018. ISBN 978-3-96147-157-7.

Band 314: Felix Tenner

Kamerabasierte Untersuchungen der Schmelze und Gasströmungen beim Laserstrahlschweißen verzinkter Stahlbleche (LDS)

LPT, xxiii u. 184 Seiten, 94 Bilder, 7 Tab.
2018. ISBN 978-3-96147-160-7.

Band 315: Aarief Syed-Khaja

Diffusion Soldering for High-temperature Packaging of Power Electronics

FAPS, x u. 202 Seiten, 144 Bilder, 32 Tab.
2018. ISBN 978-3-87525-162-1.

With advances in the new generation semiconductor materials and ever-increasing requirements for reliable power electronic modules at elevated temperatures, a major limitation is the lack of qualified high-temperature device-level packaging. This work gives an overview of optimization and evaluation of Cu-Sn based Transient Liquid Phase Soldering (TLPS), a variant of diffusion soldering to implement as a high-temperature die-attach technique for power electronics production with high level of flexibility and customization. The TLPS interconnects with enriched η-Cu6Sn5 Intermetallic phase bondline were realized successfully with optimized temperature profiles. A comprehensive analysis was performed on the process-related issues of voids for the selected soldering technique and warpage for components of varying dimensions and metallizations. Further the quality of the produced joints was evaluated by thermo-mechanical loading followed by the characterization of thermal and mechanical stability. The applicability is checked with product and technology case studies and an outlook is given with comparison of the investigated production concepts.

ISBN 978-3-96147-162-1

9 783961 471621

FAU UNIVERSITY PRESS 2018